Volume 1: FUNCTIONAL SPECIFICATION
Part 2: THE BASIC 903 COMP UTER UNIT
Section 2: WORD FORMAT AND INSTRUCTION CODE
Contents
Page
Chapter 1: INTRODUCTION
1.1 General ..... 1
Chapter 2: WORD FORMAT
2.1 General ..... 2
2. 2 Representation of Numbers ..... 2
2. 3 Representation of Instructions ..... 2
2. 4 Coded form of instruction. ..... 3
Chapter 3: INSTRUCTION CODE
3. I Instruction Table. ..... 4

## Chapter 1: INTRODUCTION

## 1. 1 General.

The 903 is a conventional stored program computer operating in the parallel binary mode. In the computer each word of information consists of an 18-bit binary pattern which may represent either an instruction or an operand of an instruction (e.g. a constant).

The accumulator (A-register) usually holds the result of executing an instruction, and this result is then available as one of the operands for the next instruction. For some purposes - chiefly during the arithmetic functions of multiplication and division - the less significant end of the accumulator is extended by the addition of the 17 most significant bits of the $Q$ register, to hold a 35 -bit operand.

Instructions are stored and obeyed sequentially and without gaps. A number of registers apart from A may be used while instructions are being obeyed. Some registers are accessible to program and they are dealt with fully in Section 1.2.1; those not accessible to program are dealt briefly in Section 1.2.1. and explained fully in Part 1 of Volume 4.

## Chapter 2: WORD FORMAT

### 2.1 General.

The binary bits of a word are referred to as bits 18, 17,
16........3, 2, 1 , bit 1 being the least significant.

## 2. 2 Representation of Numbers.

When a word represents a number, bit 18 is the sign bit and indicates whether the number following is positive or negative; the binary point is placed immediately after bit 18. Numbers are represented as fractions and when bit 18 is zero the following 17 bits represent a positive number; when it is 1 a negative number is represented. Positive numbers are represented by the appropriate digits of bits 17-1 being set to 1 , and negative numbers are represented inversely in "two's complement" form.

The value that may be attributed to each digit of a
word is as follows:

$$
\begin{aligned}
& \text { Bit no. } 18,17,16 \ldots \ldots \ldots \ldots . . .3,2,1 \\
& \text { Value }-1,2^{-1}, 2^{-2} \ldots \ldots \ldots . .2^{-15}, 2^{-16}, 2^{-17}
\end{aligned}
$$

Thus the largest positive number that may be represented is:

$$
\begin{array}{lllllll}
0.11 & 111 & 111 & 111 & 111 & 111 & \left(1-2^{-17}\right)
\end{array}
$$

The smallest positive number is:

$$
\begin{array}{lllllll}
0.00 & 000 & 000 & 000 & 000 & 001 & \left(2^{-17}\right)
\end{array}
$$

The negative number with the largest possible modulus is:

$$
1.00000 \quad 000 \quad 000 \quad 000 \quad 000 \quad(-1)
$$

The negative number with the smallest possible modulus is:

$$
\begin{array}{lllllll}
1.11 & 111 & 111 & 111 & 111 & 111 & \left(-2^{-17}\right)
\end{array}
$$

## 2. 3 Representation of Instructions.

Instructions are of the single address type and when a word represents an instruction, its bits are grouped as follows:-

$\begin{array}{llll}\text { Bits per group } & 1 & 4 & 13\end{array}$

Bit 18 B This is the B-modifier marker and has significance as follows:-
0 - the instruction is obeyed as stored
1 - the address part of the instruction is modified by the addition of the contents of the $B$ register before the function is obeyed. The function part of the instruction remains unaltered by modification. The contents of the $B$ register must be set by program before the instruction is obeyed.

Bits 17-14 $F$ This may represent any one of the 16 functions ( 0 to 15), which specifies the operation to be carried out by the computer, normally on the contents of the store location specified by N (see Chapter 3 of this Section).
Bits 13-1 $N$ These are the address bits which may specify any one of 8192 store locations, addressable from 0 to 8191.
Therefore $N$, without modification, may address any location in the basic store unit. The B-modifier facility allows extra store to be addressed (see Section 1.3.4 for details).

## 2. 4 Coded form of instructions.

In the written form of a machine code instruction the function and address groups are represented by integers in the range 0 to 15 and 0 to 8191 respectively. If $B$-line modification is intended, a solidus (/) must be written immediately preceding the function digits.

Example:

Written Form

|  |  | B | F | N |
| ---: | ---: | :---: | :---: | :---: |
| 4 | 256 | 0 | 0100 | 0000100000000 |
| $/ 14$ | 8126 | 1 | 1110 | 1111110111110 |

Stored Binary Form
$\begin{array}{lll}0 & 0100 & 0000100000000 \\ 1 & 1110 & 1111110111110\end{array}$
1.2.2.

## Chapter 3: INSTRUCTION CODE

## 3. 1 Instruction Table.

NOTES: (1) The following symbols are used in this table:

$$
\begin{aligned}
\mathrm{p} & =\text { number of places shifted } \\
\mathrm{z} & =\text { number of words transferred } \\
\mathrm{d} r & =\text { device response time }
\end{aligned}
$$

For significance of all other symbols used in this table see Introduction to the 903 Manual.
(2) All times specified are for unmodified instructions and are subject to a $\pm 10 \%$ tolerance. For a modified instruction $7.2 \mu \mathrm{~s}$ must be added to the times specified.
(3) The obeying of any instruction in these tables means that $s:=s+1$ unless otherwise stated.
(4) If an instruction is to be modified, $q$ is altered in an undefined manner before the instruction is obeyed.

| FUNCTION | DESCRIPTION | EFFECT OF INSTRUCTION | $\begin{aligned} & \text { REGISTERS } \\ & \text { NOT } \\ & \text { AFFECTED } \end{aligned}$ | INSTRUCTION TIMES ( $\mu \mathrm{S}$ ) | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | Set B-Register | $\begin{aligned} & \mathrm{b}:=\mathrm{m} \\ & \mathrm{q}:=\mathrm{m} \end{aligned}$ | A | 29.5 | an INTERRUPT cannot take place after this ins truction. |
| 1 | Add | $\mathrm{a}:=\mathrm{a}+\mathrm{m}$ | Q,B | 23.0 |  |
| 2 | Negate and Add | $\begin{aligned} & \mathrm{a}:=-\mathrm{a}+\mathrm{m} \\ & \mathrm{q}:=\mathrm{m} \end{aligned}$ | B | 26.0 |  |
| 3 | Store Auxiliary Register | $\begin{aligned} & \mathrm{m} 18:=0 \\ & \mathrm{~m} 17-1:=\mathrm{q} 18-2 \end{aligned}$ | A, Q, B | $\begin{aligned} & 24.5 \\ & 24.5 \end{aligned}$ |  |
| 4 | Load | $\mathrm{a}:=\mathrm{m}$ | Q,B | 23.0 |  |
| 5 | Store | $\mathrm{m}:=\mathrm{a}$ | A,Q,B | 24.5 |  |
| 6 | Collate | $\mathrm{a}:=\mathrm{a} \& \mathrm{~m}$ | Q,B | 23.0 | This function generates the logical product of a and $m$ |
| 7 | Jump if a zero | Provided $a=0$, s13-1: = n <br> s16-14 unchanged <br> s18, 17 undefined <br> q undefined <br> If $a \neq 0, s:=s+1$ | A, B | If $\mathrm{a}=0,27.5$ <br> If $a>0,21,0$ <br> If $\mathrm{a}<0,19.5$ |  |
| 8 | Jump unconditionally | Whether a is negative, zero or positive (not tested), the effect is as for Function 7, except that $\mathrm{s}:=\mathrm{m}$ | A, Q, B | 23.0 |  |
| 9 | Jump if a-ve | Provided a<0, the effect is as for Function 7. If $a \geq^{0}, \mathrm{~s}:=\mathrm{s}+1$ | A, B | $\begin{aligned} & \text { If } a<0,25.0 \\ & \text { If } a \geq 0,19.5 \end{aligned}$ |  |
| 10 | Count in store | $\mathrm{m}:=\mathrm{m}+2^{-17}$ | A,Q,B | 23.5 |  |
| 11 | Store SCR | $\begin{aligned} & \mathrm{q} 18-17 \text { undefined } \\ & \mathrm{q} 16-14:=816-14 \\ & \mathrm{q} 13-1:=0 \\ & \mathrm{~m} 13-1:=813-1 \\ & \mathrm{~m} 18-14:=0 \end{aligned}$ | A, B | 30.0 | q18, q17 are undefined because s 18, s 17 are undefined |
| 12 | Multiply | $(\mathrm{a}, \mathrm{q} 18-2):=\mathrm{axm}$ <br> q1 undefined | B | 78.5 |  |

1.2.2.

| FUNCTION | DESCRIPTION | EFFECT OF INSTRUCTION | REGISTERS NOT AFFECTED | INSTRUCTION <br> TIMES ( $\mu \mathrm{s}$ ) | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 13 | Divide | $\begin{aligned} & \mathrm{a}:=\frac{a, q 18-2}{n} \pm 2^{-17} \\ & q:=\frac{a, q 18-2}{n}-2^{-\alpha 7} \pm 2^{-17} \\ & a 1:=1 \\ & q 1:=0 \end{aligned}$ | B | 79.0 | It is not in general possible to say when the result in A is greater or less than the true quotient. If, however, the quotient can be expressed exactly in 17 or fewer bits (counting from the sign digit) then the following alternatives apply:- <br> a) Divisor positive. The correct quotient is in $Q$; A contains the correct quotient plus $2^{-17}$ <br> b) Divisor negative. The correct quotient is $A+2^{-17}$; the contents of $Q$ are the correct quotient less $2^{-85}$ 。 |
| 14 | Shift <br> LeftShift <br> Right Shift | Provided 0 0 n $\$ 47$ $(\mathrm{a}, \mathrm{q}):=(\mathrm{a}, \mathrm{q}) \times 2^{\mathrm{n}}$ <br> Provided $8144 \leq n \leq 8191$ $(a, q):=(a, q) \times 2^{n^{-8192}}$ | B |  | The effect of trying to shift more than 48 places is not defined. <br> The sign bit is regenerated. |
|  | Block transfer Block input | Provided 2048 $\leq n \leq 4095$ <br> Transfer x words from the peripheral device specified by bits n11-1 into store locations y to $\mathrm{y}+\mathrm{x}-1$ $y=a$ $x=q 12-1$ (i.e. $x \leq 4095$ ) If $x=0$ the instruction has no effect. | B | $23.5+(7+d r) z$ | Before the instruction is issued A must contain the address of the first location to which data is to be input. q12-1 must specify the number of locations to which data is to be input. On completion of the instruction, A contains the last word input. |
|  | Block output | Provided 4096<n<6143 <br> Transfer x words to the peripheral device specified by bits n11-1 from store locations $y$ to $y+x-1$ $y=a$ $x=q 12-1$ (i,e, $x \leq 4095$ ) If $\mathrm{x}=0$ the instruction has no effect. | B |  | Before the instruction is issued A must contain the address of the first location from which data is to be output. q12-1 must specify the number of locations from which data is to be output, One completion of the instruction, A containg the last word output. |


| FIPMCTION | DESERIPTION | EPFECT OF INSTRUCTION | $\begin{aligned} & \text { REGISTERS } \\ & \text { NOT } \\ & \text { AFFECTED } \end{aligned}$ | INSTRUCTION TIMES ( $\mu \mathrm{s}$ ) | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 15 | Input <br> Input information from peripheral device |  |  | $20.5+\mathrm{dr}$ |  |
|  |  | Provided $0 \leq n \leq 2047$ a:= one 18 -bit word from the device specified by bits n11-1 | Q,B |  |  |
|  | Input from <br> 'Tape Reader' | Provided $n=2048$, a shifted left 7 places a8-1: = 8-bit character input from tape reader | Q,B |  | If both al=0 before left shift takes place, and bit 8 of character read by tape reader $=0$, $\mathbf{a 8} 8=0$; if a 1 was a one, bit 8 of the character read by tape reader $=1$ m16-14 are ignored |
|  | Input from Teleprinter | Provided $n=2052$, a shifted left 7 places a8-1:=8-bit character input from teleprinter | Q,B |  |  |
|  | Output <br> Output information to peripheral device | Provided 4096 $\leq n \leq 6143$ one 18 -bit word output from $A$ to the device specified by bits n11-1 | Q,B | 19.04 dr |  |
|  | Output <br> information <br> to Tape <br> Punch | Provided $n=6144$ a8-1 output to paper tape punch | Q.B |  |  |
|  | Output information to Teleprinter | Provided $\mathrm{n}=6148$, a 8-1 output to teleprinter | Q,B |  | m16-14 are ignored |
|  | Program terminate | Provided $7168 \leq n \leq 8191$ <br> current program <br> level is terminated. | To be explained in Section 1.2 .4 of this manual | 19.0 | The effect of this instruction on $S$ will be explained in Section 1.2 .4 of this manurl. |

903
1.2.2.

This order code encompasses that of the MCD 920A computer. The following features are extensions to the 920A instruction code:

Block input
Block output
Preservation of $Q$ by instructions 6 and 8 .

