Functional Specification of 902 and 905

Fast Autonomous Transfer Unit

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1. Introduction

This specification defines the Fast Autonomous Transfer Unit for 902 and 905 and supersedes the report No.322 PPR 104. The Multiplex Interrupt Unit is now a separate Unit, described in 322 PPR 145.

2. Function Specification of 905 Fast A.T.U.

2.1. Introduction

The A.T.U. permits up to 6 peripherals to transfer words autonomously to and from the store. Connections between the peripherals and the A.T.U. use the 900 Series Autonomous Interface (which is similar to the 900 Series Peripheral Interface). An A.T.U. is connected to the Computer Store Highway and to Direct Input-Output Interface of the Computer. Up to four A.T.U.'s can be connected to one computer allowing the connection of up to 24 automonous peripherals. A direct channel is also available from the A.T.U. for connection of a direct peripheral.

The unit has hardware address register counter and output data register for each peripheral channel.

2.2. Sequence of Operations

A sequence of transfers to and from a peripheral is initiated by an instruction obeyed by the processor. Thereafter the sequence proceeds autonomously (unless a terminate sequence instruction is obeyed), until all transfers specified have been completed. If the peripheral is then ready for a new sequence of transfers the A.T.U. may interrupt the processor. See Fig 4 for a flow chart of A.T.U. operations.

The sequence can consist of any or all of the following:-

(a) o to 3 control word transfers to peripheral.

(b) 0 to 4095 data word transfers to or from peripheral.

(c) A status word transfer from peripheral.

2.2.1. Channel Priorities

At the end of each store cycle the peripheral channel signals are examined and the peripheral having the highest priority (i.e. connected to the lowest numbered channel) is serviced. In this way transfers on each channel may be interleaved.

2.2.2. Store Locations

Each peripheral attached to the A.T.U. has associated with it four locations in the store; the contents of these are used in the sequence of transfers as detailed below. The actual locations assigned to each peripheral are defined in paragraph 2.4.2.

Location	Bits	Function
P	1-17	Data Pointer
	18	Output Indicator
P + 1	1-12	Data Count
	15	Cyclic Indicator
	13-14	Control Count
	16	Status Word Indicator
	17-18	(spare)
P + 2	1-17	Control Pointer
P + 3	1-18	Status Word

The hardware count and address registers are automatically loaded from store when a sequence is initiated; the count register is loaded from location P + 1 and the address register from location P+2. At the start of the data transfer part of the sequence the address register is loaded automatically from location P. (If no control outputs are required the address register is loaded from P when the transfer is initiated.)

2.2.3 Cyclic Operation

At the end of data transfer if bit 15 of the count register is a 1 the address and count registers are automatically re-loaded from locations P + 1 and P, and the data transfer part of the sequence thus repeated. The loop is broken when the peripheral raises CONTROL READY in place of DATA READY thus causing a termination see (2.5.1)

2.3. Control of Transfers

Control Word Transfers take place from store locations whose addresses are given by the contents of the address register, this register is incremented each time a control word is transferred so that words may be transferred from consecutive store locations. The number of control word transfers in a sequence is controlled by bits 13 and 14 of location P+1; these bits represent a count of the number of control words to be transferred as follows:-

Bits 14	Bit 13	No. of transfers
1	1	3
1	0	2
0	1	1
0	0	0

During the last word of a control word transfer LAST WORD is not sent to the peripheral.

Data Transfers take place to or from locations whose addresses are given by the contents of the address register. This register is incremented each time a data word is transferred so that words are transferred to or from consecutive store locations. Bit 18 of location P is a one to indicate output and a zero to indicate input. The number of data words transferred is controlled by bits 1-12 of location P + 1; if the number represented by these bits is X the number of words to be transferred is X. The count register is decremented each time a data word is transferred. When the count register = 0 no further data transfers take place.

During the last word of a data transfer a Last Word Signal is sent to the peripheral to indicate the end of the sequence.

A Status word input takes place if bit 16 of location P + 1 is a one; The status word is placed in location P + 3.

2.4 Program Control

As previously mentioned, each peripheral may cause an interrupt if it is ready for a new sequence. These interrupts are connected to an interrupt "patch" connector so that they may be linked to interrupt extension inputs. These inputs are connected together to produce an interrupt, normallyon level 3. Instructions are provided to enable or inhibit interrupts on the interrupt extension inputs by means of a mask register and to determine which channel originated the interrupt. The Interrupt is cancelled by an Initiate Sequence instruction.

2.4.1. Instructions

15	5279 + N	Initiate sequence on channel N (N = 1 to 6)
15	5311 + N	Terminate sequence on channel N (N = 1 to 6)
15	5248	Allow interrupts on interrupt extension inputs as indicated by ones in Accumulator bits 1-12.
15	5249	Prohibit interrupts on interrupt extension inputs as indicated by ones in Accumulator bits 1-12
15	1152	Place status of interrupt extension inputs into bits 1-12 of Accumulator.
15	1153	Place into Accumulator bits 1-4 identification number of interrupt extension input causing interrupt. If more than one source of interrupt is simultaneously present the source connected via the patching connector to the lowest interrupt extension is indicated, the Accumulator is cleared if no interrupts are present.
15	1183 + N	Place Address Register of channel N (N=1-6) into the accumulator, including output indicator.
15	1215 + N	Place Count Register of channel N (N = 1-6) into the accumulator, including status and cyclic indicators.
15	1157-59	Undefined.
15	5252-55	Undefined.

The mask register is cleared (i.e. all interrupts are inhibited) when the computer is reset.

When the Terminate Sequence instruction is obeyed it immediately stops transfers of any type on the specified channel.

When more than one A.T.U. is used the interrupt signal from the second is treated as an external signal for the first, and so on for subsequent units. Instructions referring to the second, third and fourth A.T.U.'s have 8, 16 and 24 respectively added to all the above addresses.

2.4.2 Store Locations

	Channel No.					
	1	2	3	4	5	6
Data pointer	32	36	40	44	48	52
Indicators	33	37	41	45	49	53
Control pointer	34	38	42	46	50	54
Status word	35	39	43	47	51	55

For the second, third and fourth A.T.U.'s 32, 64 and 96 respectively are added to the above addresses.

2.5 Interfaces and Connections

2.5.1 A.T.U. to Peripheral Interface

The Interface lines provided are listed below together with the equivalent 900 Series Direct Interface lines.

Autonomous Interface	Direct Interface
Data in 1 - 18	Data in 1 - 18
Data out 1 - 18	Data out 1 - 18
Address 1	Address 1 - 2
-	Addresses 3 - 7
	Addresses 8 - 11
Input select	Input select
Output select	Output select
Reply	Reply
-	Block transfer
Last Word	Last word
-	Interrupt 1
Data ready	Interrupt 2
Control ready (useoptional)	Interrupt 3

Autonomous Interface	Direct Interface
Reset	Reset
Power On	Power On
-	Auto
-	Mains failure
Mask	-

Since each channel is separately controlled the Autonomous Interface signals are unique to each channel, (e.g. during input on a channel it does not matter what is occurring on the other channel input lines).

The 'ready' lines are used by each peripheral to initiate a transfer. 'Data ready' initiates either a transfer of a Data word or of a control word. 'Control ready' can only initiate a status input or control output transfer. If 'Control ready'is made true during a data input or output sequence when a 'Data ready' is expected it causes premature termination of the sequence. When it occurs the next transfer is a Status Word Input (if the Status Word Indicator is true.). The one bit cyclic indicator register is also cleared.

The mask line is intended to inform the peripheral that it is connected to an Autonomous Interface and not the Direct Interface. Address bits 2 - 11 are always zero on an ATU interface. Address bit 1 denotes Data Input or Output if false and Control Output or status Input if true.

2.5.2. Interface Timing

Control Output

If the next transfer on a particular channel is a control output, the 'control ready' and the 'data ready' signals are examined at the end of the store cycle. If either 'ready' is true and the channel has highest priority (ie is the lowest numbered channel) the next store cycle is assigned to that channel. When information is available, from the store, it is loaded into the data register (one for each channel), and 'output select' is made true. Thereafter the peripheral responds by making 'reply' true and then false when 'output select' returns false.

Data Output

If the next transfer on a particular channel is a data output the sequence is similar to that for control output above except that only 'data ready' can initiate the sequence.

Data Input

If the next transfer on a particular channel is a data input, 'input select' is made true when 'data ready' is made tuue. When the peripheral responds with 'reply' the next store cycle is assigned to that peripheral (provided it has highest priority). At the end of the store cycle 'input select' is made false hence the peripheral mades 'reply' false.

Termination

When the data word count is zero the ATU inputs device status if status word indicator is true. In this case 'input select' is made true when either 'control ready' or 'data ready' is made true, and the sequence proceeds as for Data Input above.

If the Status Word Indicator is false or when Status has been input the ATU waits for the next 'ready', either 'Data or Control', and passes this on to the processor as an Interrupt, via the Interrupt 'Patching' connector.

Note. If 'control ready' is made true when a 'data ready' is expected during a data transfer sequence the termination sequence is entered immediately regardless of the data word count.

The 'data ready' signal is ignored when 'input select' or 'output select' is made true until 'reply' is made false, hence the 'data ready' signal should have been made false before reply is made false if the peripheral is not immediately ready for another transfer. The 'control ready' signal should always be made false before 'reply' is made false.

2.5.3. Sockets A and B

The central processor to ATU peripheral interface is regenerated and connected to SKTA and SKTB. SKTA contains all the direct peripheral signals listed above whilst SKTB only contains:-

Output Select	Reply
Address 1 & 7-11	Ready Y
Data Out 1 and 2	Reset
Power on	Mains failure

SKTB is intended for the control of devices connected directly on the store bus (ie disc and drum controllers).

2.5.4. Interrupt 'Patching' Connector

The individual interrupts (generated by either 'ready' signal at the start of a new sequence) are grouped on an additional connector; this enables the allocation of leads and priorities to be 'patched' if necessary, and additional external signals connected where desired. The signals available on the connector and the standard connections are as follows:-
One of the select A.TU. lines are linked to Ov if the A.T.U. is the second, third or fourth A.T.U. respectively.

From	To
Mains Failure - Processor	-
Interrupt Channel 1	Interrupt Extension I/P 4
Interrupt Channel 2	Interrupt Extension I/P 5
Interrupt Channel 3	Interrupt Extension I/P 6
Interrupt Channel 4	Interrupt Extension I/P 7
Interrupt Channel 5	Interrupt Extension I/P 8
Interrupt Channel 6	Interrupt Extension I/P 9
Ready Y (skt B)	Interrupt Extension I/P 10
-	Interrupt Extension I/P 11
-	Interrupt Extension I/P 1
-	Interrupt Extension I/P 2
-	Interrupt Extension I/P 3
Interrupt 3 from other units	Interrupt Extension I/P 12
Interrupt Extension Output	Interrupt 3 - to processor
Interrupt 1 from other units	Interrupt 1 - to processor
Interrupt 2 from other units	Interrupt 2 - to processor
Ov	-
-	Select A.T.U. NO.2
-	Select A.T.U. No.3
-	Select A.T.U. No.4

If any interrupt extension input is made one a one will be generated on; the interrupt extension output provided that the corresponding bit of the mask register has been set.

It should be noted that when the A.T.U. channel 'readys' are examined for priority at the end of each store cycle channel 1 still has the greatest priority, no matter what connections are made on the patching connector, the connection only affects the priority of interrupt sources in the 15 1153 instruction.

2.6. System Configuration

Figure 1 shows the connection of the A.T.U. into a 905 system. It will be seen that a direct interface extension socket is provided to avoid the use of a multiplexer when another A.T.U. or other direct device is attached. This socket is identical to a 900 Direct Interface socket except that the 'interrupt 3' signal is routed to the interrupt patching connector and is normally connected as an external interrupt signal.

2.7. Performance (Fig 3)

The time for operations with a 1 μ sec. store is as follows:-

The maximum speed of transfer is 1.2 to 2.2. μ sec plus the peripheral response time to positive and negative 'select' signals.

	ready→1 to Select→1	reply→ 1 to Select→0	Reply→0 to Select→1 if Ready = 1
Control Output) Data Output)	1 μ sec.* to 2 μ sec.	0.2 μ sec.	1 μ sec. * to 2 μ sec.
Data Input Status Input	0.2 μ sec.	1 μ sec. * to 2 μ sec.	0.2. μ sec.

On low priority channels the times marked * are increased by the delay caused by higher priority channel operation. For 2 μ sec. store times marked * are 2 μ sec. to 3 μ sec.

2.8. Options

The A.T.U. can be supplied in 1 to 6 channel versions.

For Arch 9050 systems the logic which prohibits or allows interrupts by program control can be omitted and the channel interrupt signals routed via the Interrupt Patching Connector to the Arch Scanner. This performs identical control functions.

3. Functional Specification of A.T.U. (902)

3.1. Introduction

The Autonomous Transfer Unit for 902 is functionally similar to that for 905. Differences between the two are listed in this section. Only one A.T.U. can be connected to a 902 allowing up to four peripherals to transfer words autonomously to and from the store.

3.2. Mode of Operation

As for 905 except that the contents of the store locations associated with each peripheral are as follows -

Location	Bits	Function
P	1-12	Data pointer
P+1	1-12	Data count
P+2	1-3	Store zone indicator
	4-5	(spare)
	6	Output indicator
	7	Cyclic indicator
	8-9	Control count
	10	Status word indicator
	11-12	(spare)
P+3	1-12	Control pointer/status wo

The status word when input over-writes the control output pointer in location P + 3.

Bits 1-3 of location P + 2 specify the 4096 word zone of the store used for data and control transfers: blocks of words to be transferred must be in one store zone.

3.4. Instructions and addresses

3.4.1. 902 Instruction

15	1	71+N	Initiate sequence on channel N (N = 1 to 4)
15	1	75+N	Terminate sequence on channel N (N = 1 to 4)
15	0	6	Place status of interrupt extension inputs into bits 1 - 12 of Accumulator.
15	0	7	Place into accumulator bits 1-4 identification number of interrupt extension input causing interrupt. If more than one source of interrupt is simultaneously present the source connected via the patching connector to the lowest numbered interrupt extension is indicated, the accumulator is cleared if no interrupts are present.
15	1	6	Allow interrupts on interrupt extension inputs as indicated by ones in the accumulator.
15	1	7	Prohibit interrupts on interrupt extension input as indicated by ones in the Accumulator.
15	0	71+N	Read channel N Address Register
15	0	75+N	Read channel N Count Register

3.4.2. Store Locations

	Channel No.			
	1	2	3	4
Data pointer	168	172	176	180
Data count	169	173	177	181
Indicators	170	174	178	182
Control pointer/status word	171	175	179	183

3.5. Interfaces and connections

The interface to peripherals is identical to that of the 905 except that 12 data bits each way are provided. Figure 2 shows the connection of the A.T.U. into a 902 system.

There is an Interrupt 'Patching' connector as in 905 ATU except for limitation of 4 interrupt channels and no ATU selection.

3.6. Performance

As for 905 A.T.U.

3.7. Options

The A.T.U. can be supplied in 1 to 4 channel versions.

For Arch 105 systems the logic associated with program interrupt control etc. can be omitted and the channel interrupt signals routed to an Arch interrupt scanner which performs identical control functions.

4. A.T.U. Test Facilities

4.1. Engineers test and monitor facilities

These consist of -

(a) A switch having positions 'on line' and 'test'. In the former position all other test switches are disabled.

(b) For each channel an 'inhibit' switch which when operated prevents the transmission of select signals to the peripheral and inhibits reception of all signals from that peripheral.

(c) A 'store interface inhibit' switch which inhibits transmission and reception of data highway signals by the A.T.U. and causes simulated 'accept' and 'store busy' signals to be produced automatically.

(d) A two position 'normal/single cycle' switch and a 'restart' button to allow the A.TU. to be operated one store cycle at a time.

(e) A set of 12 or 18 monitor lamps and selector switches to allow the contents of the A.TU. buffer register and other signals to be monitored.

(f) A channel select switch and three push buttons to allow simulated 'ready' and reply signals to be produced.

(g) A parity and lock-out error switch having Display/Staticise/Stop positions. In 'display' the A.T.U. runs normally but the parity and lockout error lines are monitored by a lamp. In the 'staticise' position any error is staticised and displayed whilst in the 'stop' position the A.T.U. stops when an error occurs. The error is cleared by the 'restart' button in d) above.

4.2. Off-line program testing

A special cableform is used to connect the direct peripheral connector of the A.T.U. to the channel under test. Program instructions allow the simulation and monitoring of transfers. The following instructions are used for off-line test facilities on the 905.

	905 Instruction		Effect
Check I.P./O.P. STATUS OF CHANNELS.	15	1154	Monitor peripheral signals as follows:- Bits 1-6 Output Select on channels 1-6. Bits 9-14 Input Select on channels 1-6.(These signals are not monitored via the interface.)
Check Control Words.	15	1155	Monitor peripheral signals on chan as follows:- Bit 1 Address Bit 1 Bit 2 Last Word Bit 3 Input Select Bit 4 Output Select (Bits 5-18 Undefined)
Indicate Condition of Periph.	15	5250	Generate ready signals on channel as follows:- Bit 1 Make Data Ready True Bit 2 Make Data Ready False Bit 3 Make Control Ready True Bit 4 Make Control Ready False
Read From.	15	1156	Monitor data output signals on channel.
Write To.	15	5251	Set input signals on channel according to Accumulator contents.

'Reply' is made true when either a 15 1156 or 15 5251 instruction is obeyed and false when 'select' is made false. The second, third and fourth A.T.U.'s have 8, 16 and 24 respectively added to the above addresses.

The following instructions are used for off-line test facilities, on the 902.

902 Instruction			Effect
15	0	12	Monitor peripheral signals as follows:- Bits 1-4 Output Select on channels 1 - 4. Bits 9-12 Input Select on channels 1-4. (These signals are not monitored via the interface).
15	0	13	Monitor peripheral signals on channel as follows:- Bit 1 Address Bit 1 Bit 2 Last Word Bit 3 Input Select Bit 4 Output Select (Bits 5-18 undefined)
15	1	12	Generate ready signals on channel as follows:- Bit 1 Make Data Ready True Bit 2 Make Data Ready False Bit 3 Make Control Ready True Bit 4 Make Control Ready False
15	0	14	Monitor data output signals on channel.
15	1	13	Set input signals on channel according to Accumulator contents

'Reply' is made true when either a 15 1 13 or 15 0 14 instruction is obeyed and false when 'select'

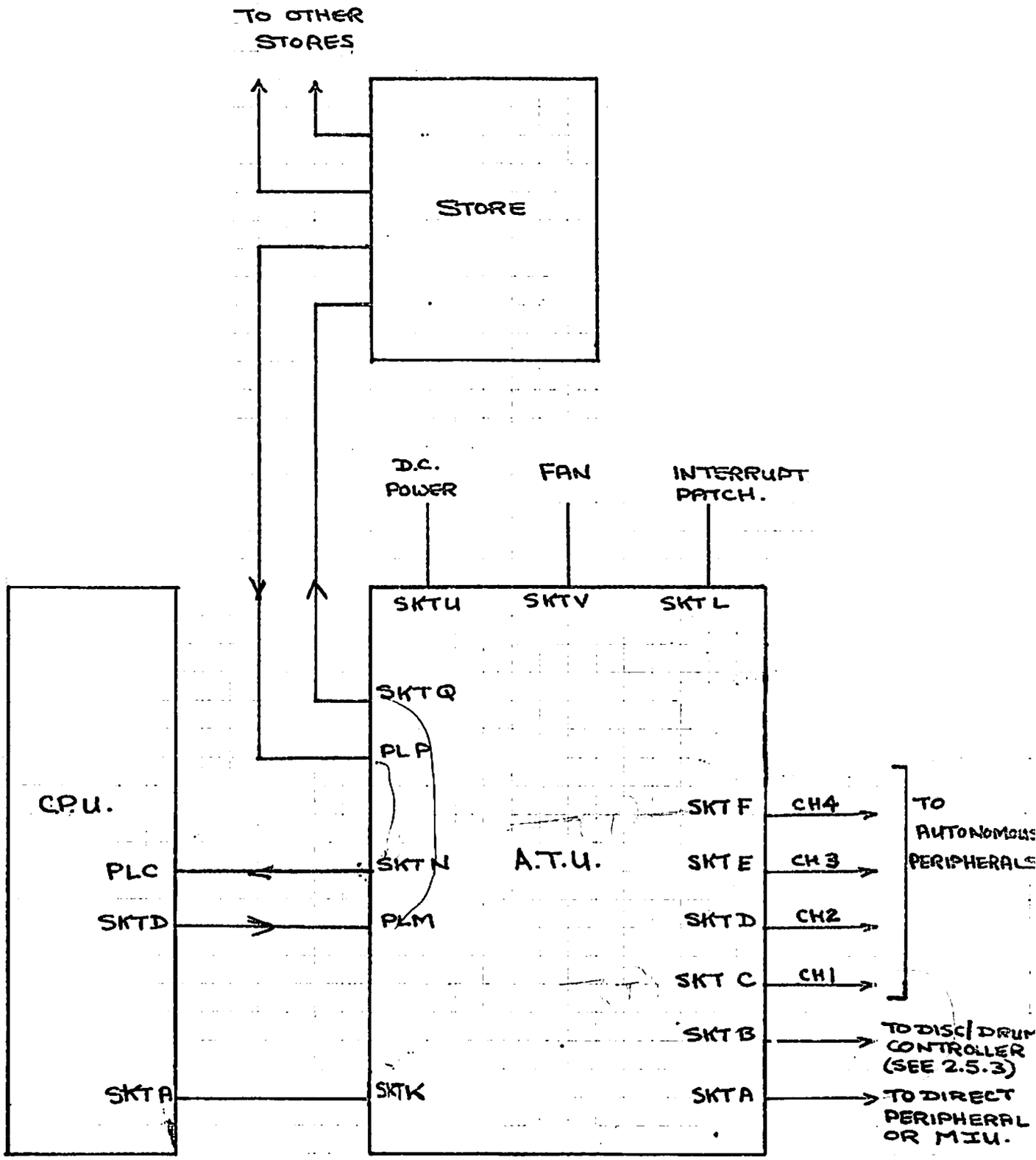
5. Mechanical construction

The unit here defined is constructed from standard plug-in boards mounted in a standard 19 inch rack mounting chassis 10½ inches high.

6. Catalogue Items

It is proposed to catalogue the units as follows:-

902	905	Item
MC2/50B	MC5/50B	A.T.U. 1 channel
MC2/50C	MC5/50C	A.T.U. additional 1 channel
MC2/50D	MC5/50D	Interrupt Logic



HOUR METER.

H
M - - - - Q P N M L K
VU - - - F E D C B A

POSITION OF CONNECTORS ON REAR OF RACK.

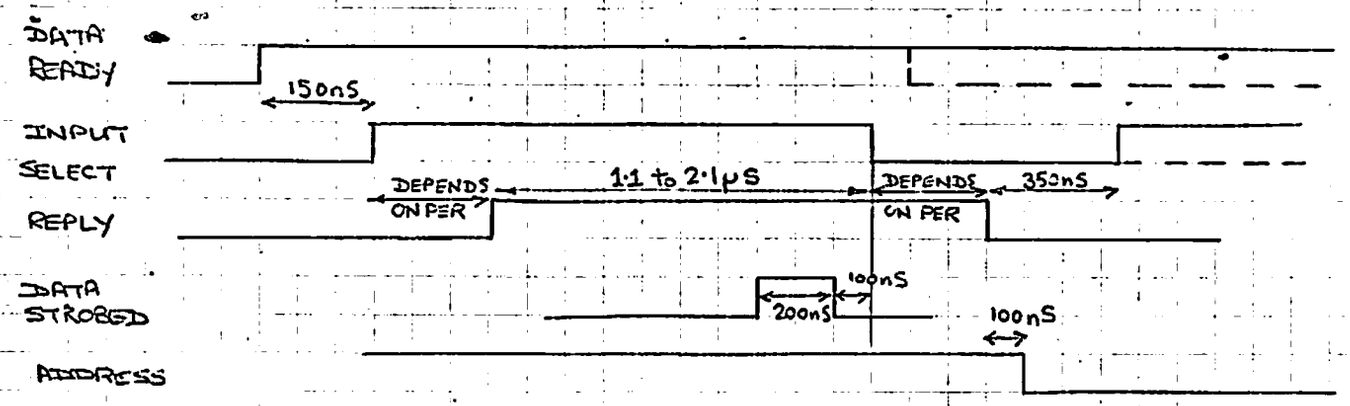
Fig. 2.

902 SYSTEM

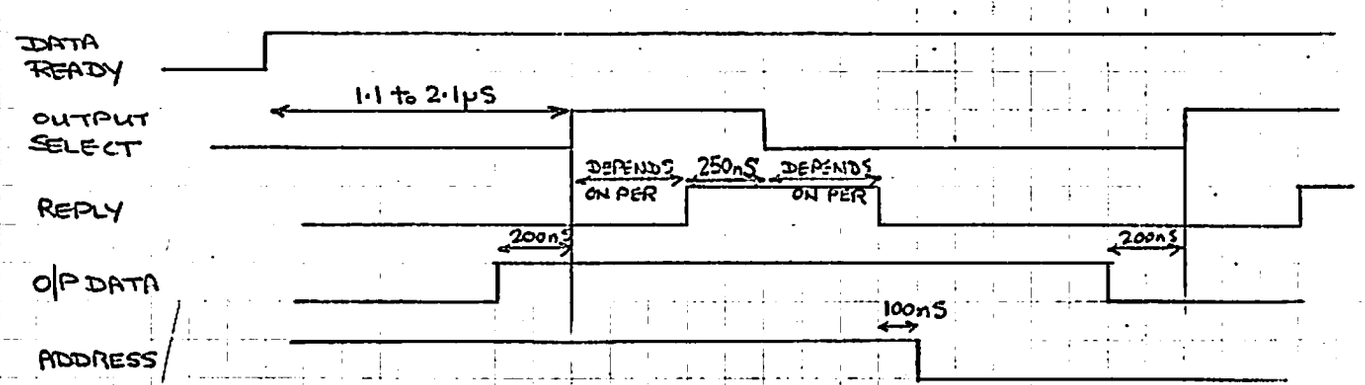
WITH AN AUTONOMOUS TRANSFER UNIT.

322 PPR 144 ISSUE B.

I/P TIMING.



O/P TIMING.



NOTE:- THESE TIMINGS ARE NOMINAL.

FIG 3 D.T.U. TIMING.