ELLIOTT

mobile computing division

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MCS 920C computer

Specification

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MCS 920C COMPUTER

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Engineering Specification

Contents

MCS 920C Computer

CENTRAL PROCESSOR MCC 4

SPECIFICATION

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1. GENERAL DESIGN

1.1 Introduction

This specification covers the MCS 920C Central Processor, wide temperature range, Catalogue No. MCC 4.

1.2 Design

1.2.1 Standard and Non Standard Parts

The equipment is supplied as a proprietary article. The electric components are either manufacturers' standard items or bought to Purchase Specifications from suppliers approved by the Mobile Computing Division of Elliott Brothers (London) Limited (M.C.D.).

1.2.2 Use of Materials, Component Parts, Dissimilar Metals

The unit is constructed with components and materials which do not support combustion and are resistant to fungus growth. Where materials of other than corrosion-resistant types are used, suitable protection is applied to resist corrosion during service as specified herein. Dissimilar metals are not used in intimate contact unless suitably protected against electrolytic corrosion. Where the assembly of any such combination of dissimilar metals is necessary, a material compatible with each is interposed.

1.2.3 Manufacturing Drawings

Final manufacturing drawings in general conform with:-

DEF 33: Preparation of Drawings for Service Requirements

B.S. 308: Engineering Drawing Practice

B.S. 530:)
) Graphical symbols (where applicable)
B.S. 3939)

Build standard is controlled by manufacturing to Drawings Lists giving full details of issues and modifications. Serial numbers of units are recorded against Drawings Lists used.

1.2.4 Design Specification

The following specifications have been used as a design basis for this unit:

DEF-5000, BS2G100, DEF-133, AvP24, AvP25, AvP970

Where this Equipment Specification and the above specifications differ the Equipment Specification shall govern.

1.2.5 Reliability

The calculated reliability indicates an MTBF of greater than 11,000 hours.

1.3 Physical Characteristics

1.3.1 Weight

Maximum weight of the unit is 20 lb.

1.3.2 Dimensions

The dimensions of the unit are:-

Length	17"	(43.2 cm.)
Width	5"	(12.7 cm.)
Height	7.5"	(19.0 cm.)

1.3.3 Mounting

The unit is designed for fitting to a frame which may be mounted in a standard 19" rack, in any attitude. The most preferable attitude (when functioning) is with cooling air passing vertically through the unit.

1.3.4 Cooling

The unit requires an external supply of cooling air of 1.45 lb./minute mass flow.

1.3.5 Marking

Marking of the internal sub-assemblies is in accordance with the manufacturer's specification.

1.3.6 Finish

The external surface of the unit is painted to Specification DEF 1059; matt black.

1.4 Electrical Characteristics

1.4.1 Radio and Compass Interference

The unit is not vulnerable to radio interference when installed with the Power Units supplied by MCD. (In these Power Units the power input lines are suppressed to above 70 dB over the range 50 Kc/s to 1000 Mc/s and above 40 dB over the range 10 Kc/s to 50 Kc/s). All relevant interconnecting cables supplied by MCD are screened to minimise radiated interference.

1.4.2 Electrical Power

Computer power inputs are derived from a Computer Power Supply Unit. Average power consumption of the central processor is 50 watts.

The regulated voltage supplies required for the unit are:-

+ 5V ± 2% at 8.5 amps.

- 6V ± 2% at up to 0.5 amps.

1.4.3 Fusing

The computer is not fitted with fuses.

1.4.4 Power Interlocks

An interlock signal to the processor becomes true when all other temperature and Power Supplies Correct signals have cleared, i.e. become true. Only when this interlock signal is true will the processor start computing (See 2.2.4.2).

1.4.5 Earthing

DC power and signal reference is to 0V (Signal Earth) which is not connected to chassis. 0V and chassis earth are brought out to separate pins in the external connectors.

Note: To obviate earth loop problems when a peripheral with its own power supply is included in a 920C system, the system should be earthed only via the mains earth connection on the peripheral's power supply unit.

1.5 Environmental Capability

1.5.1 General

The 920C central processor (MCC 4) is designed to meet most requirements of military service. Conditions in aircraft, ships and land vehicles were taken into account when defining the all-round environmental performance. In general, the design is based on Specification DEF-133 Class L2 (Ground Equipment, partially protected) and Class A2 (Airborne equipment, high flying).

1.5.2 Temperature Range

The unit will operate within specification over the temperature range 0° C to +55° C.

1.5.3 Type Approval Testing

This section defines the series of type-approval tests which the unit is designed to meet. In most cases they exceed the maximum "in-service" conditions to ensure that there is an adequate design margin. The schedule of tests is based on DEF-133 "Climatic, Shock & Vibration Testing of Service Equipment", Category A.2. The parameters specified below and the clauses of DEF-133 fully define the tests.

(a) Visual examination (DEF-133 6.1)

A function test should be made.

(b) Resonance search (DEF-133 8.1 Test A)

To Fig. 7, curve D. The unit is required to function during test.

(c) Vibration Functional (DEF-133 8.2 Test A)

To Fig. 7, curve D. The unit is required to function during test.

(d) Vibration Endurance (DEF-133 8.3 Test C and G2)

To Fig. 7, curve D. The unit is required to function during these tests.

(e) Acceleration (DEF-133 9.1)

Proof acceleration 6.5 g. The unit is required to function after test.

(f) Acceleration (DEF-133 9.2)

Non functioning test. To be applied along each of the major axes of the unit.

(g) High Temperature/Low Pressure (DEF-133 12.3)

Temperature of +55° C and pressure of 280 mm. Hg for 16 hours. The unit is required to function to DEF-133.

(h) Low Temperature Exposure (DEF-133 12.1 (B))

The unit is not required to function after test.

(i) Dry Heat (DEF-133 11.0 Test A)

Excluding measurement of surface temperatures. The computer is required to function during the test.

(*j) Low Temperature/Low Pressure (DEF-133 12.2 Test (B))

Increase temperature until chamber and unit stabilise at 0°C, when the unit is required to function.

* 4 cycles

(*k) Damp Heat (DEF-133 11.1)

Functioning during test.

* 4 cycles

(l) Tropical Life (DEF-133 11.2)

28-day test with a functioning test applied after 14 days and at the conclusion of the test.

(m) Mould Growth (DEF-133 11.3)

Non functioning test.

(n) Corrosion, Salt (DEF-133 14.0)

Functioning during test.

(o) Corrosion, Acid (DEF-133 14.1)

Functioning during test.

(p) Corrosion, Alkaline (DEF-133 14.2)

Functioning during test.

(q) Contamination (DEF-133 14.3)

Functioning test to be carried out after end of test.

(r) Dust and Sand (DEF-133 10.0)

Functioning during test, unaffected by presence of dust and sand.

(s) Toppling (DEF-133 7.4)

The unit shall stand on either of its narrowest faces and be made to topple three times onto either of its broadest faces. The test shall be carried out without covers fitted. At the conclusion of the test the unit will be required to function satisfactorily.

(t) Drop (DEF-133 7.1)

One drop from 1" on to each of the corners. At the conclusion of the test the unit is required to function satisfactorily.

(u) Bump Test (DEF-133 7.0 Test A)

The unit will be required to function satisfactorily at the conclusion of this test.

1.6 Life

The unit has no life limiting components. Shelf life is considered to be a minimum of 5 years.

1.7 Performance Standard

The performance standard is established, before delivery, to the relevant Elliott "Post Commissioning Check" procedure.

1.8 Maintenance

1.8.1 Lubrication

There is no requirement for lubrication on the unit.

1.8.2 Special Tools

Due regard has been given to holding the requirement for special tools to a minimum and to use tools currently available to the service organisations operated by the customer. The following are essential:-
Hand unwrapping tool, Gardner-Denver No. 505084 (L.H.)
Wire wrap gun, Gardner-Denver No. 14R2, mandrel No. 500350, Bit No. 500353.
Spanners, 4-40 UNC and 6-32 UNC.

1.8.3 Interchangeability

All items having the same part numbers and modification level are directly and completely interchangeable with respect to the performance and installation of the unit.

1.8.4 Periodic Re-calibration

There is no requirement for periodic re-calibration on the unit.

1.8.5 Periodic Maintenance

There is no requirement for preventive maintenance on the unit.

2. Functional Specification

2.1 Processor Performance and Capability

The 920C Central Processor (Cat. No. MCC 4) is a conventional stored program digital computer, and operates in a parallel binary mode. Its inherent capabilities and performance are detailed below. Section 2.2 details the control facilities available.

2.1.1 Word Format

In the processor, each word of information will consist of 18 binary digits, which may represent either numbers or instructions.

Numbers

In arithmetic operations the range of numbers that may be represented will be from -1 to $+(1 - 2^{-17})$. Thus bit one will have an absolute value of $+2^{-17}$, bit 2 a value of $+2^{-16}$ etc., and finally bit 18 a value of -1.

Instructions

When representing instructions the 18 bits are divided into three groups, viz: bit 1 to 13 the address N; bits 14 to 17 the function F; and bit 18 the address modifier B.

When the address modifier facility is used, the range of store locations specified by computer instructions will be increased from 8192 to 131,072 words.

2.1.2 Program Levels and Interrupt Facility

2.1.2.1 Program Levels

The processor will obey program on one of four possible priority levels. Interruption of a current program can only take place if a higher priority program level is requested. When a higher level is requested, operations on the current program will be temporarily suspended and the higher level program instructions will be obeyed. When this higher level program terminates, and providing there is no higher program level requested, the processor will revert to the lower level program and carry on from the point at which it was interrupted.

2.1.2.2 Priority Levels

Program level 1 is the highest priority and cannot be interrupted, while level 4 is the base program level and can always be interrupted by a request from any peripheral equipment.

Program level 2 can only be interrupted by level 1

Program level 3 can only be interrupted by levels 1 and 2

Program level 4 can be interrupted by levels 1, 2 and 3.

2.1.2.3 Interrupt Routine

A sequence control register (S register) and a modification register (B register) for each program level are held in particular locations in the computer store. The Address Mode Indicator (H staticisor) is also held in store (see section 2.1.7.2).

The store locations utilised are 0 to 7, and are distributed as follows:-

Program Level	S Register Location		B Register Location	H Staticisor Location	
1	0	bits 1 to 17	1	0	bit 18
2	2		3	2	
3	4		5	4	
4	6		7	6	

In order to obviate the relatively long access time of the S register, that would be experienced by the processor, an S register for the program level currently in use is held in the processor.

The contents of this register are automatically stored and replaced by previously stored values, when program interruption or termination occurs.

2.1.3 Trace Diagnostic Facility

Use of this facility simplifies the tracing of program faults or errors. The prepared TRACE program may be operated, for example, on program level 1 and the suspect program on say, level 4. A permanent interrupt is set for level 1 and the timing of the interrupt logic will be such that, when program 1 terminates, a single instruction of level 4 program will be obeyed before the processor is able to return to level 1. Thus the prepared program is obeyed after each instruction of the suspect program, and a comprehensive survey of the effect of each suspect program instruction can be obtained for examination.

The TRACE program will operate on any one of levels 1, 2 and 3 and may examine programs on any level lower than itself.

2.1.4 Initial Instructions Facility

A set of permanently available Initial Instructions will facilitate the reading of program tape from the paper tape station into the processor. These instructions will appear to be in store locations 8180 to 8191 inclusive, and will be the only means by which programs may be read into the computer in the first instance.

Provision is made whereby the first Program Terminate instruction to be obeyed will allow the contents of store locations 8180 to 8191 to be read or written into the processor (instead of initial instructions).

The initial instruction pattern is compatible with the 920 series of computers.

2.1.5 Block Transfer Facility

A single computer instruction will specify the particular peripheral from which a series of words will be transferred to a series of consecutive store locations. A similar instruction will transfer a series of words from consecutive store locations to a specified peripheral. The number of peripherals addressable is 2,047.

2.1.6 Autonomous Store Access Facility

2.1.6.1 Autonomous Access

This facility will allow information to be transferred directly between the store and certain peripherals without using the processor.

Information will be extracted from or placed in the store by "stealing" store cycles. Such data transfers will be made to interleave with normal processor computations.

Peripherals that are capable of addressing the store direct, referred to as Autonomous Access Channels, will have signal and data lines connected in parallel with the respective processor lines. There is provision for up to four channels to be so connected.

Peripherals that are not capable of addressing the store direct may acquire autonomous access via the Interface Control Unit. This unit is connected to one of the four data bus outlets mentioned above, and in turn will accomodate up to sixteen peripheral devices on its outlet system.

2.1.6.2 Priority Levels

Control logic in the processor will determine the allocation of priorities for the use of the bus system, giving preference to external autonomous access channels requiring to transfer data to or from the store. The logic will examine the four possible 'request' signals to the autonomous access channels, and will send an 'accept' signal to the channel having the higher priority, enabling it to perform one complete store cycle.

Channel 1 shall have the highest priority and will be accepted first. Channel 2 will be accepted in the absence of a request from Channel 1. Channel 3 will be accepted in the absence of requests from Channels 1 and 2. Channel 4 will be accepted in the absence of requests from Channels 1, 2 and 3.

The processor will only be able to access the store in the absence of channel requests.

2.1.7 Store Addressing

2.1.7.1 Relative Addressing

The store will comprise individual blocks of 8192 words each, and in order to place a number or instruction in any available location, the particular store as well as its location must be contained in the address.

This relative form of addressing is obtained by adding bits 14-17 of the S register to the N bits (1-13) for all functions except 14 and 15. Thus the N bits will specify the location, and the S register bits will specify the store block in which the location is situated. Two other forms of store addressing are given below.

2.1.7.2 H. Mode Address

The store will comprise individual blocks of 8192 words each, in which numbers or instructions may be placed in any location of any available block. The N bits of an instruction will be interpreted according to the state of Address Mode Indicator (H) and the function (F) being obeyed.

If H=1 and for functions 0 to 6 and 10 to 13, then the N bits will specify absolutely a location in the first block of store (0 to 8191), i.e. absolute addressing.

If H=0 and for functions 0 to 13, then the N bits will specify a location in which the instruction is itself located, and bits 14-17 of the S register will specify the store block in which the location is situated. Thus the relative address of the location will be formed by adding the N bits to digits 14-17 of the S register, as in 2.1.7.1.

2.1.7.3 B Modified Address

The range of store locations which may be specified by an instruction can be increased to 131,072 words, by adding the contents of the B register to the unmodified address. This modification of the address will be effected by making B (bit 18) of the instruction, one.

The addition of the B register contents and the unmodified address bits will be executed prior to implementing the instruction, only the least significant 17 bits being used.

The instruction held in the store location will not be affected by this process.

2.1.7.4 Store Addressing Summary

The address of a store location may be defined by a number M, calculated as follows:

Function	B = 0 H = 0	B = 0 H = 1
0 - 6) 10 - 13)	$M = N + S_{14-17}$	$M = N$
7 - 9	$M = N + S_{14-17}$	$M = N + S_{14-17}$
14 - 15	$M = N$	$M = N$

Function	B = 1 H = 0	B = 1 H = 1
0 - 6) 10 - 13)	$M = B + N + S_{14-17}$	$M = B + N$
7 - 9	$M = B + N + S_{14-17}$	$M = B + N + S_{14-17}$
14 - 15	$M = (B + N)_{1-13}$	$M = (B + N)_{1-13}$

2.1.8 Processor Instruction Code

The 18-bit word, when used to represent instructions, is made up of 1 modifier bit, 4 function bits and 13 address bits.

A comprehensive instruction code containing up to 67 functions is realised by extending the effect of the four function bits in the following ways:-

(a) By direct use of certain addresses with the 14 and 15 functions to specify different "addressless" instructions, or instructions which require only a small part of the full address range. * .

(b) By giving certain functions secondary effects which do not interfere with the primary effect but are nevertheless extremely useful.

(c) By taking advantage of the fact that the modifier registers of all four program levels (including the one currently active) and the sequence control register, accumulator and auxiliary register of the three program levels not currently active are held in the computer store and can be addressed as for any other store location.

* Note that for functions 14 and 15 only the 13 least significant bits of N are meaningful where N is the absolute value.

The resulting instruction set of 67 instructions is given in the following tables.

Notes Terms used in the following tables are defined briefly below:-

A Register	An accumulator with a capacity of 18 bits which holds the results of the computations prior to output transfer.
B Register	Holds the 18 bit modifying number for modifying the store address.
H Staticisor	Is the Address Mode Indicator, which allows bits 14-17 of the S Register to specify the store block in which a location is required.
N	The absolute address specified by an instruction, modified or un-modified.
Word Generator	18-bit word generator situated in the Control and Monitor Unit, which may input numbers to the A Register.
Q Register	Has a capacity of 18 bits and can be used to hold information during computation, or as an extension to the accumulator. In the latter use, the least significant end of the A Register is extended by 17 bits.

A, Q	Represents a double length number stored in both Registers, used as one.
S Register	Has a capacity of 17 bits and controls the extraction of instructions from the store. It is incremented after each instruction is obeyed and thus contains the address of the next instruction to be obeyed.

a represents contents of the accumulator (A)

b represents contents of the modifier register (B)

h represents the state of the address mode indicator (H)

q represents contents of the Q Register (Q)

q^{2-18} represents contents of the auxiliary register

s represents contents of the sequence control register (S)

n represents contents of location N.

Any letter followed by ' represents the new contents of the appropriate register or store location.

2.1.8 TRANSFERS BETWEEN REGISTERS AND STORE

Instruction	Effect	Function and Address Representation	Specification
Set A	$a' = n$	4 N	Place the contents of the store location specified by N in the accumulator.
Set B	$b' = n$	0 N	Place in the B register of the current program level, the contents of the store location specified by N. This instruction places the same information in the Q register.
Set Q	$q' = n$	0 N or 2 N	Place in the Q register the contents of the store location specified by N. If instruction 0 is used the same information is placed in the B register, but the accumulator is not affected. If instruction 2 is used, the B register is unaffected but (n-a) is placed in the accumulator.
Store A	$n' = a$	5 N	Place the contents of the accumulator in the store location specified by N.
Store S	$n'_{1-13} = s_{1-13}$ $q'_{14-17} = s_{14-17}$	11 N	Place bits 1-13 of the sequence control register of the current program in the store location specified by N, setting bits 14-18 of this location to zero. Place bits 14-17 of the sequence control register in the Q register, setting the remaining bits of Q to zero.

Instruction	Effect	Function and Address Representation	Specification
Store Aux.	$n'_{1-17} = q_{2-18}$	3 N	Place the contents of the auxiliary register in the least significant 17 bits of the store location specified by N. The most significant bit of the store location is made zero.

INTER-REGISTER TRANSFERS

Instruction	Effect	Function and Address Representation	Specification
A to B	b' = a	15 7174 (also 5, 1 or 3 or 5 or 7 according to current program level)	Place contents of accumulator in B register of current program level.
A to Aux.	$q'_{2-18} = a_{1-17}$	15 7172	Place bits 1 to 17 of accumulator in the auxiliary register, setting $Q_1 = 0$.
B to Q	q' = b	0 1 or 3 or 5 or 7 according to current program level	Place contents of B register of current program level in the Q register.
S to B	$b'_{1-13} = s_{1-13}$ $q'_{14-17} = s_{14-17}$	11 1 or 3 or 5 or 7 according to current program level	Place bits 1 to 13 of the sequence control register of the current program level in any B register, setting bits 14-18 to zero. Place bits 14-17 of the sequence control register in the Q register, setting the remaining bits of Q to zero.
B to A	a' = b	15 7175 (also 4, 1 or 3 or 5 or 7 according to current program level)	Place the contents of B register in the accumulator.

Instruction	Effect	Function and Address Representation	Specification
Aux. to A	$a'_{1-17} = q_{2-18}$	15 7173	Transfer contents of auxiliary register to bits 1 to 17 of the accumulator. Set bit 18 of the accumulator to zero.
Aux. to B	$b'_{1-17} = q_{2-18}$	3 1 or 3 or 5 or 7 according to current program level	Place the contents of the auxiliary register in the least significant 17 bits of any B register, making the most significant bit of the B register zero.

ARITHMETIC BETWEEN ACCUMULATOR AND STORE

Instruction	Effect	Function and Address Representation	Specification
Add n to a	a' = n+a	1 N	Add the contents of the store location specified by N to the contents of the accumulator.
Subtract a from n	a' = n-a	2 N	Negate the contents of the accumulator and add the contents of the store location specified by N. The contents of N are also placed in the Q register by this function.
Multiply a by n	(a aux)' = axn	12 N	Multiply the contents of the accumulator by the contents of the store location specified by N, and place the result in the accumulator and the auxiliary register.

Instruction	Effect	Function and Address Representation	Specification
Divide (a aux) by n	$a'_{2-18}=(a\ aux)/n$ $a'_1 = 1$	13 N	Divide the contents of the accumulator and the auxiliary register by the contents of the store location specified by N and place the result in the accumulator, making the least significant bit a one so that it is correctly rounded to 17 bits. The result is also placed in Q, with the least significant bit a zero.
Collate a with n	a' = a&n	6 N	Place ones in the accumulator in only those bit positions in which both the contents of the accumulator and the contents of the store location specified by N are ones.

ARITHMETIC BETWEEN ACCUMULATOR AND MODIFIER REGISTER

Instruction	Effect	Function and Address Representation	Specification
Add b to a	a' = b + a	1 1 or 3 or 5 or 7 according to current program level	Add the contents of the B register of the current program level to the contents of the accumulator.
Subtract a from b	a' = b - a	2 1 or 3 or 5 or 7 according to current program level	Negate the contents of the accumulator and add the contents of the B register of the current program level. The contents of B are also placed in the Q register by this function.

Instruction	Effect	Function and Address Representation	Specification
Multiply a by b	(a aux)' = a x b	12 1 or 3 or 5 or 7 according to current program level	Multiply the contents of the accumulator by the contents of the B register of the current program level, and place the result in the accumulator and the auxiliary register.
Divide (a aux) by b	$a'_{2-18}=(a\ aux)/b$ $a'_{1}=1$	13 1 or 3 or 5 or 7 according to current program level	Divide the contents of the accumulator and the auxiliary register by the contents of the B register of the current program level, and place the result in the accumulator, making the least significant bit a one so that it is correctly rounded to 17 bits. The result is also placed in Q, with the least significant bit a zero.
Collate a with b	a' = a&b	6 1 or 3 or 5 or 7 according to current program level	Place ones in the accumulator only in those bit positions in which both the contents of the accumulator and the contents of the B register of the current program level are ones.

JUMPS

Instruction	Effect	Function and Address Representation	Specification
Jump if zero	If a = 0 then $s'_{1-13}=N$ $s'_{14-17}=s_{14-17}$	7 N	If the contents of the accumulator are zero, place N in the sequence control register of the current program level.

Instruction	Effect	Function and Address Representation	Specification
Jump	$s'_{1-13}=N$ $s'_{14-17}=s_{14-17}$	8 N	Place N in the sequence control register of the current program level.
Jump if negative	If a < 0 then $s'_{1-13}=N$ $s'_{14-17}=s_{14-17}$	9 N	If the contents of the accumulator are negative, place N in the sequence control register of the current program level.
Skip if standardized	If a is standardised, then s' = s + 2	15 7169	Skip the next instruction if the contents of the accumulator are standardized (i.e. if $a \geq +\frac{1}{2}$ or $a < -\frac{1}{2}$ or a = 0).

Increment B and skip if B = 0	b' = b + 1
	if $b'_{1-13}=0$ then
	s' = s + 2
	If $b'_{1-13} \neq 0$ then
	s' = s + 1
		15 7170	Increment B register by $+2^{-17}$ and skip the next instruction if bits 1 to 13 of the result are zero.

INTERLEVEL INSTRUCTIONS

Any instruction which refers to a store location can also be used to refer to another level's sequence control register, modifier, accumulator or auxiliary register. Strictly this adds 48 possibilities (12 instructions referring to store, each of which can refer to any of the 4 stored registers). All these are not of general value, but 23 warrant inclusion.

Note: It may not be safe to refer to a priority level higher than the one currently active.

The asterisk * indicates the register of another priority level, the corresponding store location being as follows:-

S * is location 0, 2, 4 or 6 according to level
B * is location 1, 3, 5 or 7 according to level
A * and Aux * are locations allocated by the programmer.

Instruction	Effect	Function Representation
A to A *	a*' = a	5
A to B *	b*' = a	5
A to Aux*	aux*' = a	5
A to S*	s*' = a	5
A* to A	a' = a*	4
B* to A	a' = b*	4
Aux* to A	a' = aux*	4
S* to A	a' = s*	4
B* to B	b' = b*	0
S* to B	b' = s*	0
S to S*	$s*'_{1-13} = s_{1-13}$	11
Add A* to A	a' = a* + a	1
Add B* to A	a' = b* + a	1
Add Aux* to A	a' = aux* + a	1
Add S* to A	a' = s* + a	1
Subtract A from A*	a' = a* - a	2
Subtract A from B*	a' = b* - a	2
Subtract A from Aux*	a' = aux* - a	2
Subtract A from S*	a' = s* - a	2
Collate A* with A	a' = a & a*	6
Collate B* with A	a' = a & b*	6
Collate Aux* with A	a' = a & aux*	6
Collate S* with A	a' = a & s*	6

SHIFT DOUBLE LENGTH

Instruction	Effect	Function and Address Representation	Specification
Left shift AQ	$(aq)'=aqx2^N$	14 N Where $0 \leq N \leq 36$	Shift the double-length contents of A and Q left N places (multiply by 2^N)
Right shift AQ	$(aq)'=aqx2^{-N}$	14 8192-N Where $1 \leq N \leq 36$	Shift the double-length contents of A and Q right N places (divide by 2^N)

ADDRESS MODE INSTRUCTIONS

Instruction	Effect	Function and Address Representation	Specification
Set relative addressing	h' = 0	15 7176	This instruction sets the Address Mode Indicator H for the current program level to zero. When H = 0, or with functions 7, 8 or 9 the N bits of an instruction specify a location of the block in which the instruction itself is located, i.e. bits 14-17 of the S register are added to N to give the absolute address of the location.
Set absolute addressing	h' = 1	15 7177	This instruction sets the Address Mode Indicator H for the current program level to one. When H = 1 but not with functions 7, 8 or 9 the N bits of an instruction specify absolutely a location in the range 0 to 8191. This instruction also disables the initial instructions, making locations 8180 to 8191 available for normal use.

MISCELLANEOUS

Instruction	Effect	Function and Address Representation	Specification
Increment Store	$n' = n+1 \times 2^{-17}$	10 N	Increment the contents of the store location specified by N by 2^{-17}.

Instruction	Effect	Function and Address Representation	Specification
Increment Modifier	$b' = b+1 \times 2^{-17}$	10 1 or 3 or 5 or 7 according to current program level	Increment the B register of the current program level by 2^{-17}.
Read Paper Tape Character	$a'_{1-7} = t_{1-7}$ $a'_8 = t_8$ OR a_1 $a'_{9-18} = a_{2-11}$	15 2048	Read one 8 bit character from paper tape into accumulator. Shift the previous contents of the accumulator left 7 places and place the input character in the 8 least significant bits of the accumulator.
Punch Paper Tape Character		15 6144	Output the least significant 8 bits of the accumulator to the tape punch.
Block Transfer into store		14 N where $2048 \leqslant N \leqslant 4095$	Transfer n words of information from the device specified by bits 1-11 of N into store locations a to a + n -1, where a is the contents of the accumulator and n is the contents of the Q register. ($n \leqslant 4095$). The contents of A and Q are altered.
Block Transfer out of store		14 N where $4096 \leqslant N \leqslant 6143$	Transfer n words of information to the device specified by bits 1-11 of N from store locations a to a+n-1 where a is the contents of the accumulator and n is the contents of the Q register. ($n \leqslant 4095$). The contents of A and Q are altered.

Instruction	Effect	Function and Address Representation	Specification
Peripheral word input		15 N where $0 \leq N \leq 2047$	Input to the accumulator one 18 bit word from the device specified by bits 1 to 11 of N.
Peripheral word output		15 N where $4096 \leq N \leq 6143$	Output from the accumulator one 18 bit word to the device specified by bits 1 to 11 of N.
Input word generator		15 7171	Transfer the setting of the 18 word generator switches into the accumulator.
Program Terminate	$s' = s^*$ $b' = b^*$	15 7168	Terminate current program level and disable initial instructions, rendering locations 8180 to 8191 available for normal use.
Read Teleprinter	$a'_{1-7} = t_{1-7}$ $a'_8 = t_8$ OR a_1 $a'_{9-18} = a_{2-11}$	15 2052	Input one 8 bit character from the teleprinter. Shift the previous contents of the accumulator left by 7 places and place the input character in the least significant 8 bit positions of the accumulator.
Output to teleprinter		15 6148	Output the least significant 8 bits of the accumulator to the teleprinter.

2.1.9. Instruction Times

The following are typical instruction times in microseconds.

Function	Operation	Time un-modified	Time modified
0	Set B register	3.3.	4.4.
1	Add	2.2.	3.3.
2	Negate and Add	3.0	4.1
3	Store Aux. Register	3.0	4.1.
4	Read	2.2.	3.3.
5	Write	3.0	4.1
6	Collate	2.2.	3.3.
7	Jump if A zero (a $\neq$ 0)	1.1.	1.1.
	Jump if A zero (A = 0)	1.1.	2.2.
8	Jump	1.1.	2.2.
9	Jump if A negative (A $\geq$ 0)	1.1.	1.1.
	Jump if A negative (A < 0)	1.1.	2.2.
10	Count if store	3.0	4.1.
11	Store S register	3.0	4.1
12	Multiply	9.0	10.1
13	Divide	17.2	18.3
14	Shift (n places)	2.6+0.75n	3.7+0.75n
"	Block transfer (n words)	3.4+4.9n*	4.5+4.9n*
15	Input-out	4.9*	6.0*
"	Program terminate	6.7	7.8
"	Skip if standarized (no skip)	2.6	3.7
"	Skip if standardized (skip)	3.4	4.5
"	Increment B and test (B $\neq$ 0)	4.8	5.9
"	Increment B and test (B = 0)	5.6	6.7
15	Read no. gen.	3.4	4.5
"	A to Aux.	3.4	4.5
"	Aux. to A	3.4	4.5
"	A to B	3.7	4.8
"	B to A	3.7	4.8
-	Interrupt	3.3	-

Times marked * (input, output instructions) are minimum times which apply only if the peripheral responds within about 0.5 μ S.

2.1.10 Marginal Test Facility

The processor has provision for variation of its pulse timing and voltage threshold parameters, in order to determine the operational failure margin. The parameters may be varied using an external test unit, which will control the timing margins directly and control the threshold margins via the computer system power supply unit.

The processor has two logic timing groups which may be controlled by the margin test unit, either independently, or together as one group. The groups are comprised as follows:-

(a) Processor Timer;
Clock generator;
Initial Instruction Timing.

(b) Processor Stop Timing;
Write and Read Timings.

Each timing function is capable of being re-set if the result of the margin test indicates that it is necessary.

2.1.11 Control Logic Testing Facility

The processor will have provision for input of external 'forcing waveforms', which may be used to test the correct generation of most processor control logic waveforms. A total of 37 forcing waveforms and a 'check' waveform will be catered for. The latter waveform will disable the processor from operating normally, so that testing may be carried out while the processor is in a permanent control state, as directed by the particular forcing waveform being applied.

2.2 Processor Operation with Control and Monitor Unit

The processor will operate without the Control Unit connected, automatically obeying previously stored program, or program fed in from the paper tape unit, after power has been correctly applied to the system. During the period of time from the instant of switch-on and until all interlocks have cleared (indicating that power has been correctly applied) a 'Reset' signal will be applied to the processor, and transmitted over the store and peripheral interfaces.

When the Control Unit is connected to the processor, control facilities will be selective according to the position of the three-position Mode switch, as follows: -

2.2.1 Auto Mode

In the 'Auto' Mode the controls of the control unit will be inoperative, except for the power ON/OFF switch. The processor will automatically start obeying program at store location 8177, after power has been correctly applied to the system.

During the period of time from the instant of switch ON and until all interlocks have cleared, (indicating that power has been correctly applied to the system) a 'Reset' signal will be applied to the processor and transmitted over the store and peripheral interfaces.

2.2.2 Manual Mode

In this Mode, routine operation of developed programs will be enabled, controls not necessary for this function will be disabled. The effective controls available are detailed below.

After switching ON in this Mode, a continuous 'Reset' signal will be applied to the processor, and will only be cleared on the operation of the 'Jump' control.

2.2.2.1 Word Generator

The operation of the 'Jump' control causes the processor to transfer control to the program located in the store, at the address set up on bits 1-13 of the Word Generator.

The processor inputs the word set up on bits 1-18 of the Word Generator, when carrying out the program instruction "Read Word Generator".

2.2.2.2 Jump

This is a three-position control and when raised causes the processor to start obeying program on level 1 from the address set on bits 1-13 of the Word Generator keys. Depressing the control causes the processor to start obeying the initial instructions on level 1.

2.2.2.3 Stop

The operation of this button causes the processor to stop at the end of its current instruction.

2.2.2.4 Restart

Operation of this control causes the processor to restart after being stopped by the action of 2.2.2.3.

2.2.2.5 Reset

Operation of this control causes the processor to be reset, and remain in this state until terminated by the operation of 2.2.2.2.

2.2.2.6 Program Level Interrupts

An external peripheral interrupt signal on any of the three levels causes the processor either to interrupt the current program, or obey the requested program at the earliest occasion, depending upon the level of priorities.

2.2.2.6 Program Level Interrupts

An external peripheral interrupt signal on any of the three levels causes the processor either to interrupt the current program, or obey the requested program at the earliest occasion, depending upon the level of priorities.

Interrupt signals generated in the Control Unit cause the processor to operate as above.

The TRACE program can be operated on any one of levels 1, 2 and 3. The central processor will terminate the TRACE program when a permanent interrupt is set for that level, and be able to obey a single instruction of the 'suspect' program (on a lower level than the TRACE) before returning to the TRACE program level.

2.2.3 Test Mode

In this mode, testing of new programs, repair and maintenance may be carried out. All controls are operative, and those in addition to 2.2.2 that are enabled are detailed below.

After switching ON in this mode, a continuous 'Reset' signal will be applied to the processor logic and will only be cleared on the operation of the 'Jump' control.

2.2.3.1 Enter

Operation of this control causes the processor to copy the number set up by the number generator into the A Register when the 'Restart' control is depressed.

The processor will copy numbers continuously or singly, as directed by the three-position control.

2.2.3.2 Obey

Operation of this control causes the processor to obey the instruction set up by the number generator, when the 'Restart' control is depressed.

The processor will obey instructions continuously or singly, as directed by the three-position control.

2.2.3.3 Cycle Stop/Order Stop

In the 'Cycle Stop' position the processor will obey any single microprogram instruction when the 'Restart' control is depressed, and then stop.

In the 'Order Stop' position the processor will obey any single stored program instruction when the 'Restart' control is depressed and then stop.

2.2.3.4 Cycle Repeat

Operation of this control causes the processor to obey any single microprogram instruction.

2.2.3.5 Lock-Out

Operation of this control results in illuminating the 'Lock-Out' lamp and causes the processor to bring into operation the store protection facilities.

2.2.3.6 Error Stop

Operation of this control results in illuminating the 'Error Stop' lamp and causes the processor to stop if a store parity error is detected; or if the program attempts to overwrite a protected word, with store protection in operation.

2.2.4 Computer Shutdown Facility

This facility will ensure no loss or corruption of stored data and that the program terminates correctly, in the event of a system shutdown.

2.2.4.1 Conditions Initiating Shutdown

A controlled shutdown will be initiated:-

(a) by setting the Power On/Off switch situated on the control and monitor unit to the 'Off' position;

(b) if the 'Interlock' or 'Power Supply Correct' signals to the processor become false.

Condition (b) will occur if the monitored stack temperature in the store unit is not within limits, or if the sensing circuitry in the power supply unit indicates that the supply line to the processor is not within voltage limits.

A mains failure will be detected by the 'Power Supply Correct' signal going false, due to an under-voltage condition, and in this event the power supply unit will have sufficient stored energy to enable the shutdown sequence to be executed.

If the Control and Monitor Unit is not connected to the processor then condition (a) will not occur, and the system switch 'Off'/'On' operations will occur automatically under the control of the power supply unit.

2.2.4.2 Shutdown Sequence

When the 'Interlock' or the 'Power Supply Correct' signal lines to the processor become false, a 'Cycle Stop' operation similar to that obtained by operation of the cycle stop on the control and monitor unit, will immediately be effected. The processor will allow the completion of the particular microprogram instruction currently active and then stop. A second operating condition will also become immediately effective, disabling any autonomous access requests to the processor.

After a delay of 10 microseconds a continuous 'Reset' signal will be transmitted over the respective lines to the processor, store and peripherals. This 'Reset' condition will be disabled when the particular signal line returns to the true state. In the case of setting the Power On/Off switch to 'Off' (or a mains failure) the 'Reset' signal will remain true until the stored energy in the power supply unit is discharged.

3. Interface Specification

This specification describes the timing of the control and data waveforms between the central processor and the paper tape equipment, peripherals and store unit. Timing diagrams for these interfaces are given, and also a complete schedule of pin connections for all the interconnecting cables to the processor.

3.1 Peripheral Interface

Introduction

The 920C processor incorporates two input-output connectors, through which all peripheral information transfers are executed. One connector is used for the paper tape equipment and the other connector provides a general input-output 'bus' for up to four peripherals. The processor is capable of addressing 2048 peripheral devices. Timing Diagrams are shown in Figure nos. 1, 2, 3 and 4.

3.1.1 Paper Tape Outlet

Transfer of data will be in a parallel binary mode and will have a word width of 8 bits. The data rate will be: 1 character/ 4.9 microseconds.

3.1.2 General Peripheral Outlet

Transfer of data will be in a parallel binary mode and will have a word width of 18 bits. The data rate will be: 1 word/4.9 microseconds, and for block transfers will be 1 word/4.9 microseconds, when using unmodified address.

3.1.3 Data Transfer Timing

Input

When an input is required the processor will send an 'Input Select' signal to the specified peripheral. The processor will then await a 'Reply' signal before the data to be transferred will be accepted. Completion of 'data transfer' will be indicated by the absence of an 'Input Select' signal.

Output

When an output is required the processor will send an 'Output Select' to the specified peripheral. The processor will then await a 'Reply' signal before ending the transmission of the data to be transferred. Completion of 'data transfer' will be indicated by the absence of an 'Output Select' signal.

3.1.4 Interface Signals

The functions and directions of the signals on the interconnecting lines at the interface are given below. The states of lines carrying binary data are described as ONE or ZERO; and those lines carrying a logic or controlling function, as TRUE or FALSE.

Input Select/Output Select

From computer, one line each. The appropriate signal will be set to the true state to cause a word to be transferred, and will become false when the peripheral has responded. Both signals will normally be false.

Output Reply/Input Reply

To the computer, one line each. The appropriate signal will be set true to indicate when, after the appropriate select signal has become true, either output data has been accepted by the peripheral, or input data is available to the computer. Each reply signal will be set false after the appropriate select signal has become false. Both signals will normally be false.

Address Code

From computer, eleven lines. These lines carry the address bits of the selected peripheral, and will be set before the 'Select' signal goes true. The code signals will be in the correct state as long as either 'Select' or 'Block Transfer' are true; otherwise their state will be undefined.

Output Data

From computer, eighteen lines. These lines carry the bits of the word to be transferred. The lines will be in the correct state as long as 'Output Select' is true; otherwise their state will be undefined.

Input Data

To computer, eighteen lines. These lines carry the bits of the word to be transferred from the peripheral. The lines should be in the correct state when both 'Input Select' and 'Reply' are true. The lines shall not be influenced by any peripheral, other than the one that is being addressed.

Block Transfer

From computer, one line. The line will be set true before either 'Select' signal is set true, and before the first word is transferred. The line will be set false after the relevant 'Select' signal has become false, for the last word.

There is no provision for a block transfer operation to the paper tape equipment.

Last Word

From computer, one line. The line will only be set true for the last transferred word when either 'Select' signal is true. The line will be set false for any word other than the last, while either 'Select' is true. The line will be false during a single word transfer, and when 'Select' is false.

Reset

From computer, one line. The line will be set true when the computer is first switched on, and if operating in the 'Auto' mode, will become false when the various interlocks clear. On switching on in the 'Manual' or 'Test' mode, the line will be set true, continuously, until the 'Jump' control is operated. The line will also be set true continuously when the 'Reset' control is operated (in the 'Manual' or 'Test' mode) and will only become false on operation of the 'Jump' control.

The line will normally be set false, but will become true when switching off the computer, or if a line voltage or store temperature fault condition occurs.

Interrupts

To computer, three lines. Each line should normally be set false. A line should be set true by a peripheral requiring the computer to enter its program level; it should be set false again before the termination of the interrupting program.

Power On

From computer, one line. This line will be energised when power is applied to the central processor, and will be de-energised when power is removed.

3.1.5 Peripheral Transmitters and Receivers

The central processor contains transmitters and receivers that make direct connection with the signal lines interconnecting the peripheral channels with the computer.

Nominal operating parameters are given below:

3.1.5.1 Transmitter:

Loading: one cable and up to four receivers for each transmitter.
Nominal "O" level output: 0.4V at 10mA Sink
Nominal "1" level output: 3.2V at 16mA Source
Nominal output impedance: 50 ohms.

3.1.5.2 Receiver:

Nominal threshold: 2V at 25° C
Nominal "1" level input requirement: 3V at 4mA
Nominal "O" level input requirement: 0V at 0mA

3.1.5.3 Noise Margin:

With similar transmitters and receivers in the peripheral equipment and a maximum cable length of 10 feet, a nominal noise margin of one volt will be maintained over the operational temperature range.

3.2 Store Interface

Introduction

The 920C central processor is provided with two connectors through which all store information transfers are executed. One connector is used for information entering the processor and the other for information leaving the processor.

The connectors feed out to a data bus system, which can also be used for data transfers directly to autonomous access channels. Each channel may feed a peripheral capable of corresponding with the store directly; or a less complex peripheral device, via an Interface Control Unit. In either case, data is transferred without passing through the processor, and logic circuitry in the processor regulates the access to store on a priority basis.

The processor to store interface therefore contains some signal lines only relevant to the autonomous access channels.

Timing diagrams are shown in Figure Nos. 5 and 6.

3.2.1 Data Transfer

Transfer of data between store and processor will be in a parallel binary mode and will have a word width of 18 bits. The maximum data transfer rate is 870,000 words per second. Store-processor operating modes will be confined to read/restore and clear/write cycles.

Data entering the store is duplexed with the store location address, thereby reducing the number of lines involved.

3.2.2 Data Transfer Timing

3.2.2.1 Data from Store

When an input is required by the processor, it will send a 'Select Store' signal along the store line, and also the address of the store location required. A 'Trigger Read' signal and a 'Permit Write' signal will then be transmitted to the store, and the processor will await a 'Read Busy' signal from the store.

The start of data transfer from the store will be indicated by the ending of the 'Read Busy' signal. During the data transfer a 'Write Busy' signal will be sent from the store, and the ending of this signal will occur before the cessation of the data being transferred at the end of the cycle.

3.2.2.2 Data to Store

When an output is required by the processor, it will send a 'Select Store' signal along the store bus, and also the address of the store location required. The processor will then transmit 'Trigger Read', 'Permit Write' and 'Inhibit Read Out' signals to the store, and will await a 'Read Busy' signal from the store.

When the processor receives 'Read Busy', the address information will be removed from the duplexed lines and the data to be transferred substituted. During the data transfer a 'Write Busy' signal will be sent from the store and the ending of this signal will cause the cessation of the data being transferred.

3.2.3 Interface Signals

The functions and directions of the signals on the interconnecting lines at the interface are given below. The states of the lines carrying binary data are described as ONE or ZERO, and those lines carrying logic or controlling functions, as TRUE or FALSE.

Store Select

From computer, eight lines. A line when set true will allow the appropriate store unit to respond to control signals. It becomes false when the 'Address' lines are set to their zero state. Each line is normally false when the appropriate store is not being accessed.

Address and Data Output

From computer, eighteen lines. Fourteen of the lines are duplexed, carrying both the address and data information. Each duplexed line will be in its correct state for the address bits at the same time as 'Store Select', and will become zero after the start of 'Read Busy' and before the end of 'Trigger Read'.

The lines will remain zero for a short duration after transmitting the address. All eighteen lines will then be set to their correct state for the binary word to be transferred, and will remain correct until the end of 'Write Busy'.

The lines are normally in the zero state and are only set otherwise when the store is being accessed.

Trigger Read and Permit Write

From computer, one line each. Both signals will only become and remain true when 'Store Select' is true, and when the 'Address' lines are in their correct state.

The lines are normally false when the store is not being accessed.

Inhibit Read Out

From computer, one line. This line will only become and remain true, when 'Trigger Read' is true and when data is required to be written into store.

The line is normally false when the store is not being accessed.

Read Busy

To computer, one line. This line will be set true when 'Trigger Read' is true, and will become false when the 'Data Output' lines are set to their correct state.

The line is normally false when the store is not being accessed.

Write Busy

To computer, one line. This line will be set true when 'Read Busy' has become false, and during the time that the 'Data output' lines are set to their correct state. It will become false before 'Data Input' or 'Data Output' are set to their zero state.

The line is normally false when the store is not being accessed.

Data Input

To computer, eighteen lines. The lines will be set to their correct state when 'Read Busy' becomes false, and before 'Write Busy' is set true. The data input information will remain established until the end of the cycle.

The lines are normally in the zero state and are only set otherwise when the store is being accessed.

Parity Error

To computer, one line. The line will only be set true when the parity of the data information to be transferred is not correct. In such an event the signal will be set about 150 nanoseconds after the establishment of the data by the store, and will remain true until the end of the cycle.

Lock Out Error

To computer, one line. The line will only be set true if a protected location of the store is addressed, when attempting to write data into store. In such an event, the signal will be set about 100 nanoseconds after the establishment of the address information, and will remain true until the end of the cycle.

Store Reset

From computer, one line. The line will be set false when the computer is first switched on, and if in the 'Auto' mode, will become true when the various interlocks clear. On switching on in the 'Manual' or 'Test' mode, the line will be set false continuously until the 'Jump' control is operated. The line will also be set false continuously when the 'Reset' control is operated (in the 'Manual' or 'Test' mode) and will only become true on operation of the 'Jump' control.

The line will normally be set true but will become false when switching off the computer, or if a line voltage or store temperature fault condition occurs.

Lockout

From computer, one line. The line when set false will not allow protected store locations to be over-written.

The line will normally be set false, but may be set true in 'Manual' or 'Test' operating modes, whereupon data may be written into any store location.

Interlock

To computer, one line. The line will be set true when store voltage and temperature are within limits. The line will normally be true, and will only become false when a fault occurs.

Interlock In

From computer, one line. This line will be energised when power is applied to the central processor and will be de-energised when power is removed.

Autonomous Access Channel: Request

To computer, four lines. A line when set to the true state will indicate to the processor that there is an autonomous channel requiring access to store. Towards the end of each store cycle, all 'Request' signals will be examined on a priority basis to allow a store access to the data bus system.

The 'Request' signal remains true until the appropriate 'Accept' signal is received. The line is normally false.

Autonomous Access Channel: Accept

From computer, four lines. A line, when set true, will allow the appropriate autonomous channel unhindered access to store for one complete cycle.

The 'Accept' signal will remain true until the end of the cycle, and at all other times when not accessing store, will be false.

Program Level Information

From computer, two lines. The state of these lines 'E2' and 'E3', will indicate the current level of program, and are provided for a multi-programming facility.

3.2.4 Store Transmitters and Receivers

The central processor contains transmitters and receivers that make direct connection with the signal lines interconnecting the store bus system with the computer. Nominal operating parameters are given below.

3.2.4.1 Transmitter

Loading: One cable and up to eight receivers for each transmitter.
Nominal '0' level output: 0.4V at 10mA, Sink.
Nominal '1' level output: 3.0V at 50mA, Source.

3.2.4.2 Receiver

Nominal Threshold: 1.5V at 25°C
Nominal '1' level input: 3.2V at 0mA.
Nominal '0' level input: 0.45V at 1mA.

Note: The gating signal should only be applied to the receiver during the relevant cycle.

3.3. Interface Connection Details

The interconnection details between the processor and the other system units are given in the following schedules.

3.3.1 · Paper Tape/Central Processor Connection Schedule: Socket E

Processor fixed connector: Hellerman Deutsch, DSM00 12-14 SY

Cable free connector: Hellerman Deutsch, DSM07 12-14 PY 004

Computer Socket Pin	Function	Computer Socket Pin	Function
1	Tape Add 1	21	Power On
2	" 2	22	Starting Add.
3	" 3	23	0V
4	" 4	24	0V
5	Tape 0/P 1	*25	Select Punch
6	" 2	26	0V
7	" 3	27	-
8	" 4	28	-
9	" 5	29	0V
10	" 6	30	-
11	" 7	31	0V
12	" 8	*32	Select Reader
13	Tape I/P 1	33	Reply Punch
14	" 2	*34	Reply Reader
15	" 3	*35	Reset
16	" 4	o36	0V
17	" 5	37	Mains Earth
18	" 6		
19	" 7		
20	" 8		

* Single Coax cable required in cable form

o Connect to outer braid of cable form

3.3.2 Peripheral/Central Processor Connection Schedule: Plug B

Processor fixed connector: Hellerman Deutsch, DSM00 27-30 PX
Cable free connector: Hellerman Deutsch, DSM07 27-30 SX004

Computer Plug Pin	Function	Computer Plug Pin	Function
1	Periph. O/P 1	39	Periph. I/P 5
2	" 2	40	" 6
3	" 3	41	" 7
4	" 4	42	0V
5	" 5	43	Periph. I/p 8
6	" 6	44	" 9
7	0V	45	" 10
8	Periph. O/P 7	46	" 11
9	" 8	47	" 12
10	" 9	48	" 13
11	" 10	49	0V
12	" 11	50	Periph. I/P 14
13	" 12	51	" 15
14	0V	52	" 16
15	Periph. O/P 13	53	Periph. I/p 17
16	" 14	54	" 18
17	" 15	*55	Input Reply
18	" 16	56	0V
19	" 17	*57	Output Reply
20	" 18	*58	Input Select
21	0V	*59	Output Select
22	Periph. Add 1	60	0V
23	" 2	61	Block Transfer
24	" 3	62	Last Word
25	" 4	*63	Interrupt 1
26	" 5	64	0V
27	" 6	*65	Interrupt 2
28	0V	*66	" 3
29	Periph. Add 7	67	Reset
30	" 8	68	0V
31	" 9	69	Power On
32	" 10	70 - 89	Spare
33	" 11	90	Mains Earth
34	Periph. I/P 1	+91	0V
35	0V		
36	Periph. I/P 2		
37	" 3		
38	" 4		

* Single Coax cable required in cable form.
\+ Connect to outer braid of cable form.

3.3.3 Store/Central Processor Connection Schedule: Plug A

Processor fixed connector: Hellerman Deutsch, DSM00 27-30 PW

Cable free connector: Hellerman Deutsch, DSM07 27-30 SW 004

Computer Plug Pin		Function	Computer Plug Pin		Function
Signal	Return	Duplexed Store Address	Signal	Return	
1	2	and Data In, Bit 1	51	52	Trigger Read,
3	4	" 2	53	54	Permit Write,
5	6	" 3	55	56	Inhibit Read Out,
7	8	" 4	57	58	$\overline{\text{Store}}$) Store $\overline{\text{Reset}}$)
9	10	" 5	59	60	Interlock In
11	12	" 6	61	62	$\overline{\text{Lock Out}}$, Lock Out
13	14	" 7	63	64	Store Select, 1
15	16	" 8	65	66	" 2
17	18	" 9	67	68	" 3
19	20	" 10	69	70	" 4
21	22	" 11	71	72	" 5
23	24	" 12	73	74	" 6
25	26	" 13	75	76	" 7
27	28	" 14	77	78	" 8
29	30	Store Data In Bit 15	* 91		0 Volt.
31	32	" 16			
33	34	" 17			
35	36	" 18			
37	38	Autonomous Access Channel, Accept 1			
39	40	" 2			
41	42	" 3			
43	44	" 4			

Note: All connections are single coax cable, except * which is connected to outer braid of cable form.

3.3.4 Store/Central Processor Connection Schedule: Plug C

Processor fixed connector: Hellerman Deutsch, DSM00 19-33 PW

Cable free connector: Hellerman Deutsch, DSM07 19-33 SW 004

Computer Plug Pin Signal	: Return		
1	2	Store Data Out,	Bit 1
3	4	"	" 2
5	6	"	" 3
7	8	"	" 4
9	10	"	" 5
11	12	"	" 6
13	14	"	" 7
15	16	"	" 8
17	18	"	" 9
19	20	"	" 10
21	22	"	" 11
23	24	"	" 12
25	26	"	" 13
27	28	"	" 14
29	30	"	" 15
31	32	"	" 16
33	34	"	" 17
35	36	"	" 18
37	38	Autonomous Access Channel, Request	1
39	40	"	" 2
41	42	"	" 3
43	44	"	" 4
47	48	Program Level,	$\overline{E2}$
49	50	"	$\overline{E3}$
51	52	Read Busy	
53	54	Write Busy	
55	56	Interlock	
57	58	Parity Error	
59	60	Lockout Error	
* 61		0 Volts.	

Note: All connections are single coax cable, except * which is connected to outer braid of cable form.

3.3.5 Control Monitor Unit/Central Processor Connection Schedule: Socket F

Processor fixed connector: Hellerman Deutsch, DSM00 27-30 SW
Cable free connecter: Hellerman Deutsch, DSM07 27-30 PW 004

Computer Socket Pin			
1	Active 1 : Lamp	35	MAN INT 3
2	" 2 : "	36	MAN INT 2
3	" 3 : "	37	CYCLE STOP
4	0 Volts	* 38	RESTART SS
* 5	S.S. level 1	39	MAN INT 1
* 6	" 2	40	PERM INT 1
* 7	" 3	41	PERM INT 3
8	Manual or Test	42	LOCKOUT
9	Lockout Error: Lamp	43	CYCLE REPEAT
10	Parity Error: Lamp	44	OBEY
11	+5 volts	45	Word Gen, Bit 5
12	ON/OFF Switch	46	" 12
13	Return for pin 12	47	" 4
14	+5 volts	48	" 3
15	ORDER STOP	49	" 9
16	NG2	50	" 2
17	Word Gen: Bit 18	51	" 1
18	" 16	52	" 11
19	" 15	53	" 10
21	" 6	54	" 13
22	" 14	55	0 Volts
23	" 7	56	Word Gen, Bit 17
24	" 8	57-66	0 Volts
25	NG2-1	67	AUDIO
26	Ready: Lamp	68	Stop: Lamp
27	AUTO	69	Reset:Lamp
28	Power On: Lamp	70	-6 Volts
29	Demand 2: Lamp	72-76	+5 Volts
30	" 1: Lamp	81	-6 Volts
31	" 3: Lamp	83	ERROR OVERRIDE
32	ENTER	* 85	RESET S.S.
* 33	JUMP S.S.	o 90	0 Volts
34	PERM INT 2	91	Mains Earth

* Single Coax cable required in cable form.

o Connect to outer braid of cable form.

3.3.6 Control Monitor Unit/Central Processor Connection Schedule:

Socket G

Processor fixed connector: Hellerman Deutsch, DSM00 12-14 SX

Cable free connector: Hellerman Deutsch, DSM07 12-14 PX004

Computer Socket Pin	Function	Computer Socket Pin	Function
1	MON 1	26	MON T1
2	" 2	27	" T2
3	" 3	28	" C1
4	" 4	29	" C2
5	" 5	30	" C3
6	" 6	31)	0 Volts
7	" 7	32)	
8	" 8	33)	
9	" 9	34)	+ 5 Volts
10	" 10	35)	
11	" 11	*36	0 Volts
12	" 12	37	0 Volts
13	" 13		
14	" 14		
15	" 15		
16	" 16		
17	" 17		
18	" 18		
19	0 Volts		
20	MON A		
21	" Q		
22	" P		
23	" M		
24	" J		
25	" S		

* Connect to outer braid of cable form

3.3.7 Power Supply Unit/Central Processor Connection

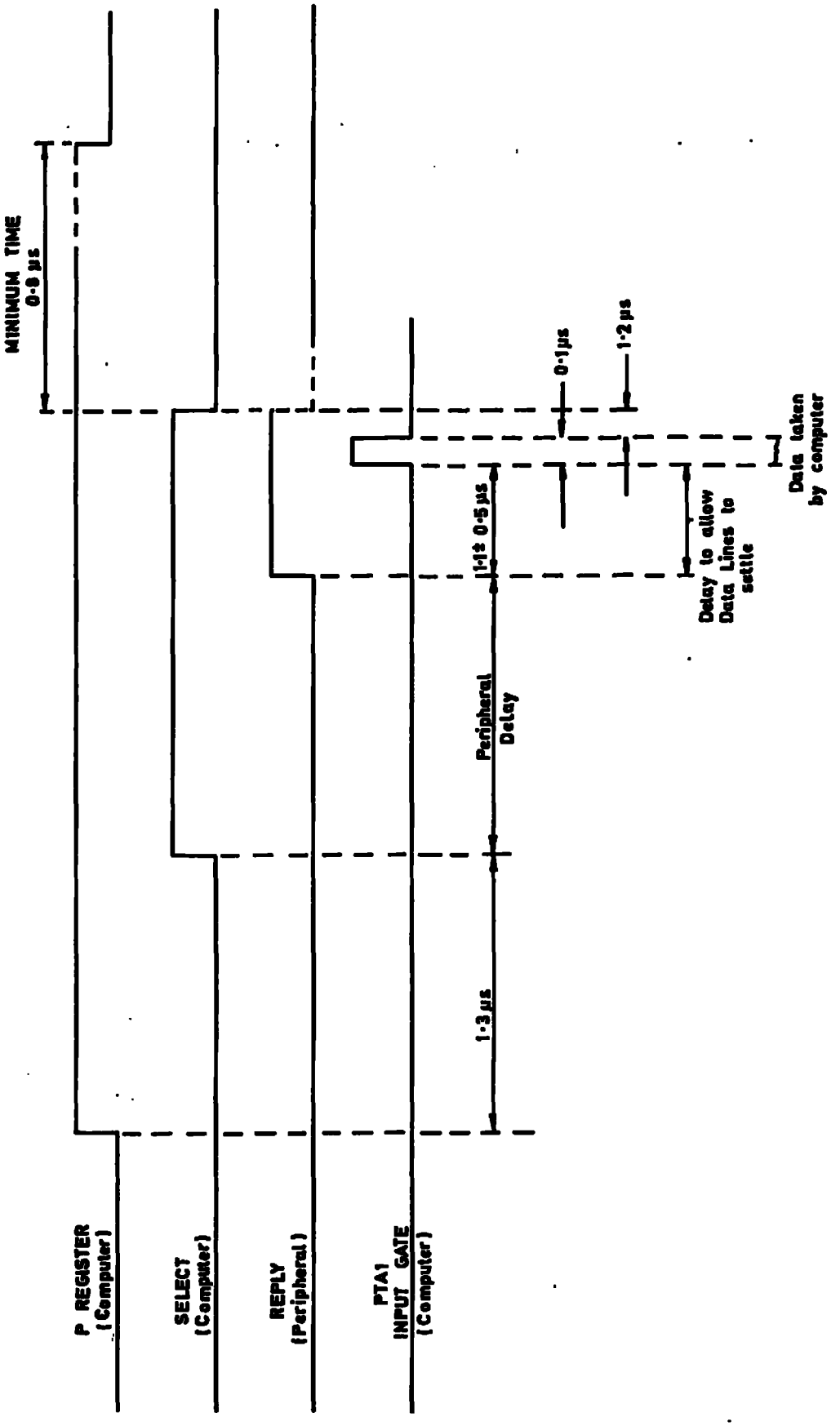
Schedule: Plug D

Processor fixed connector: Hellerman Deutsch, DSM00 27-30 PW
Cable free connector: Hellerman Deutsch, DSM07 27-30 SW 004

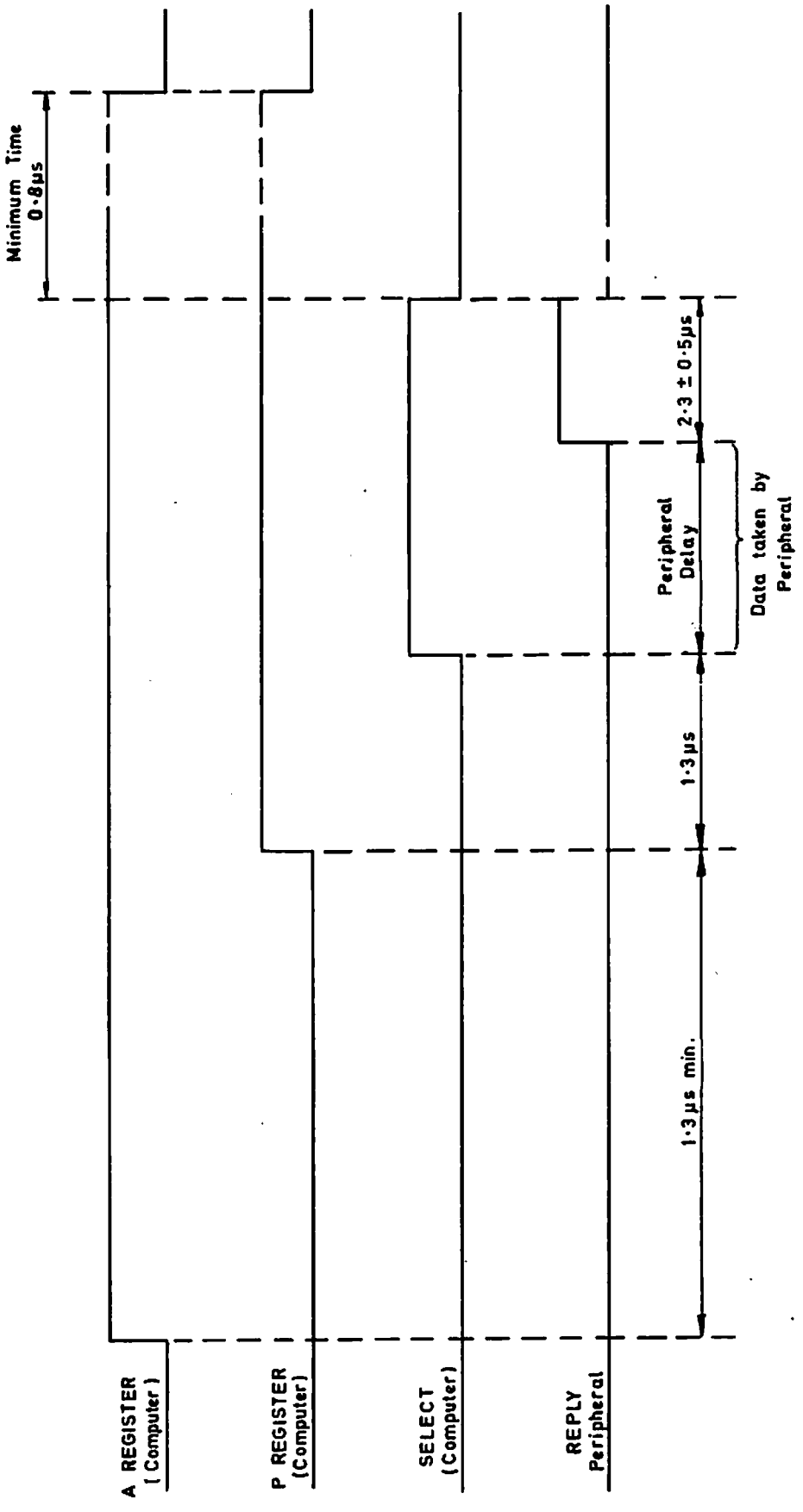
Computer Plug Pin	
1-13	+5 Volts Supply
14	POWER ON
15	Return for Pin 14
16-28	0 Volts Supply
29	-6 Volt Supply
30	Power Supply Correct
31	Return for Pin 30
32	Timing Margin, 1
33	" " 2
34	" " 3
35	Forcing Waveform, FW1
36	" FW2
37	" FW3
38	0 Volts
39	Forcing Waveform, FW4
40	" FW5
41	" FW6
42	0 Volts
43	Forcing Waveform, FW7
44	" FW8
45	" FW9
46	0 Volts
47	Forcing Waveform, FW10
48	" FW11
49	" FW12
50	0 Volts
51	Forcing Waveform, FW13
52	" FW14
53	" FW15
54	0 Volts
55	Forcing Waveform, FW16
56	" FW17
57	" FW18
58	0 Volts
59	Forcing Waveform, FW19
60	" FW20
61	Forcing Waveform, FW21
62	0 Volts
63	Forcing Waveform, FW22
64	" FW23
65	" FW24
66	0 Volts
67	Forcing Waveform, FW25
68	" FW26
69	" FW27
70	0 Volts
71	Forcing Waveform, FW28
72	" FW29
73	" FW30
74	0 Volts
75	Forcing Waveform, FW31
76	" FW32
77	" FW33
78	0 Volts
79	Forcing Waveform, FW34
80	" FW35
81	" FW36
82	0 Volts
83	Forcing Waveform, FW37
84	CHECK
85	0 Volts
86	Spare
87)	
88)	0 Volts
89)	
90)	
* 91	Mains Earth

Note:

* Connect to outer braid of cable form. Pins 35 to 85 inclusive, are concerned with the 'Control Logic Testing Facility' (see section 2.1.11.), and shall remain without connection in normal system operation.

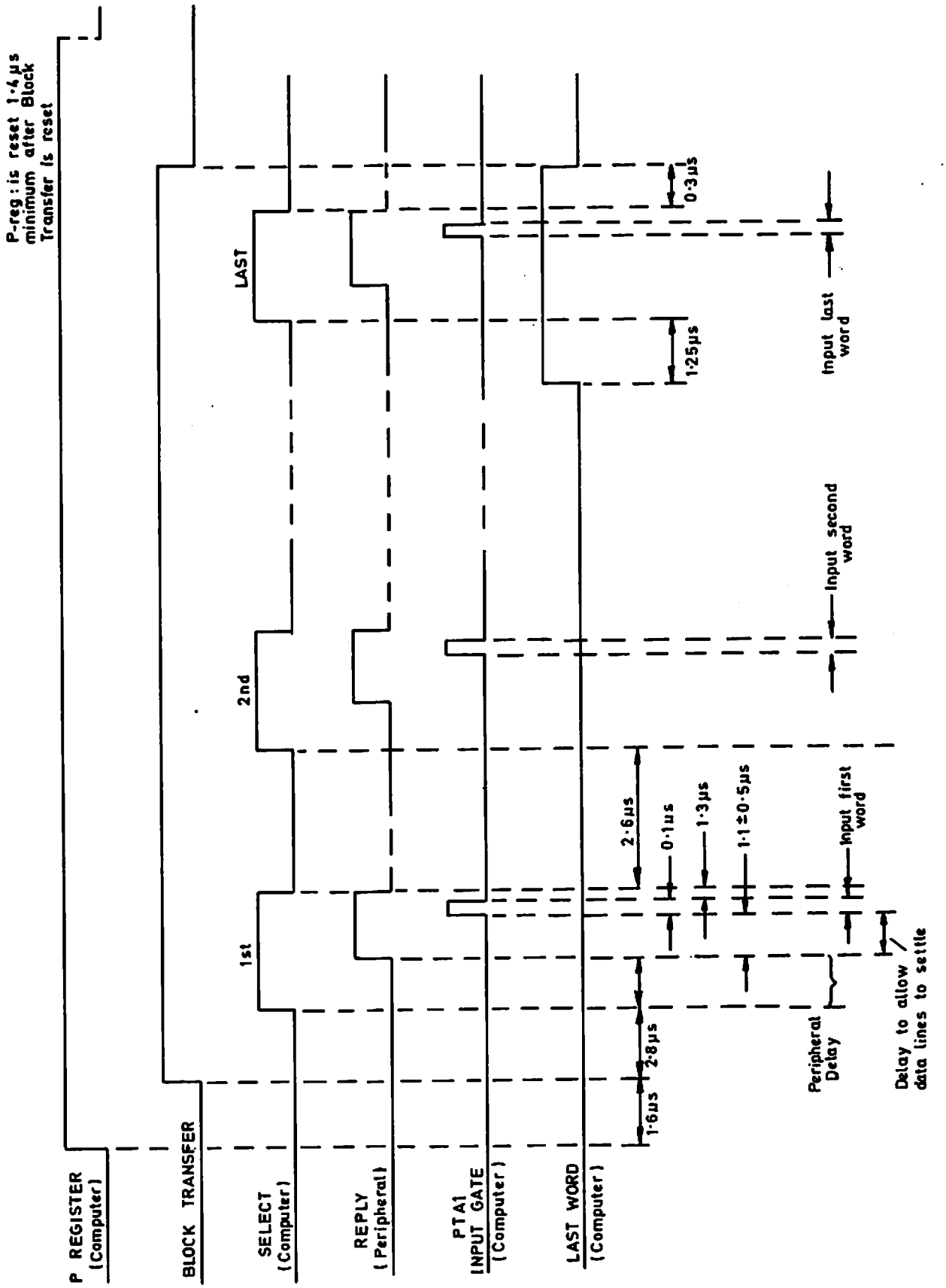


Direct Input Timing Fig. N°1



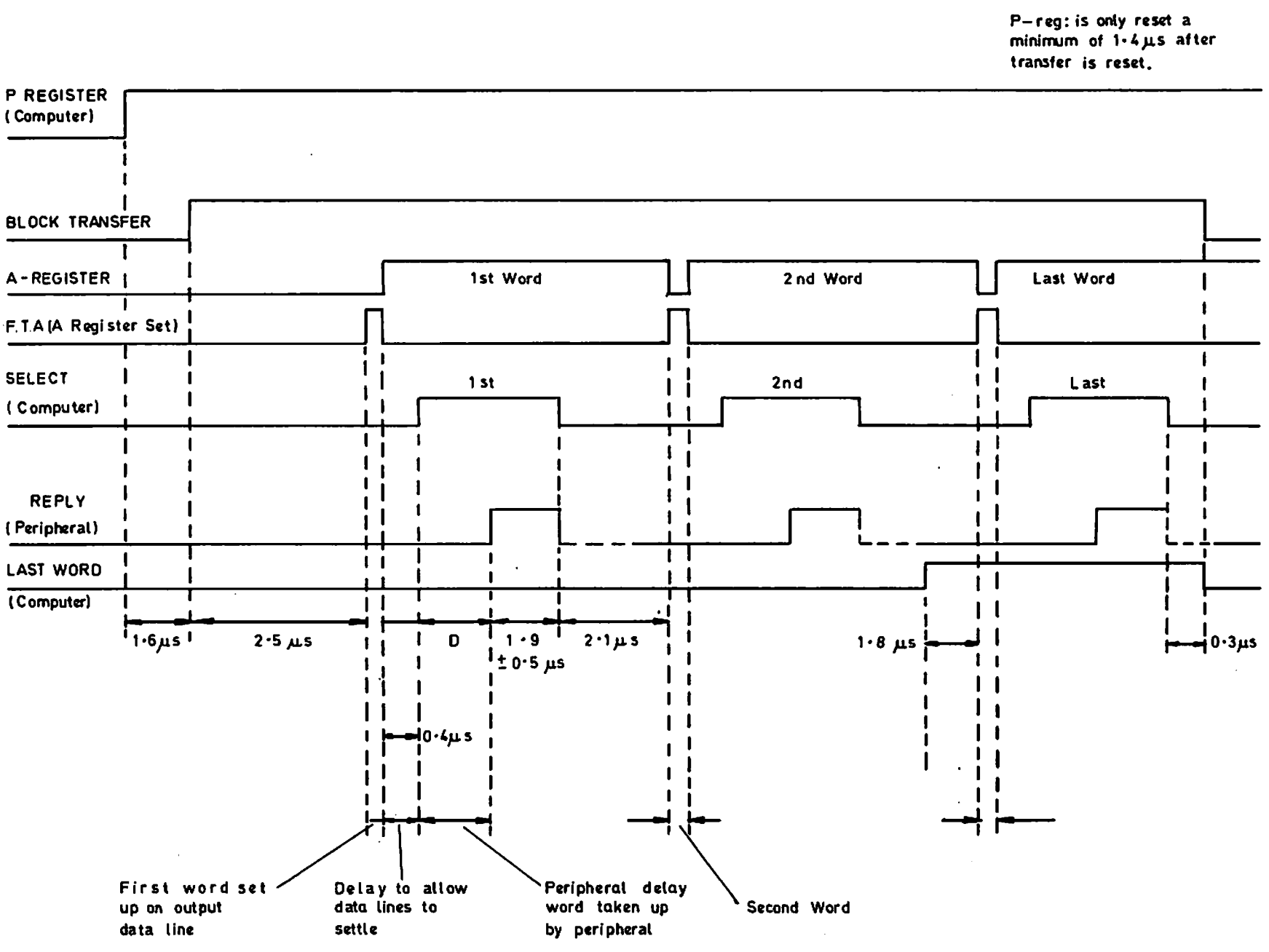
Direct Output Timing

Fig. N° 2



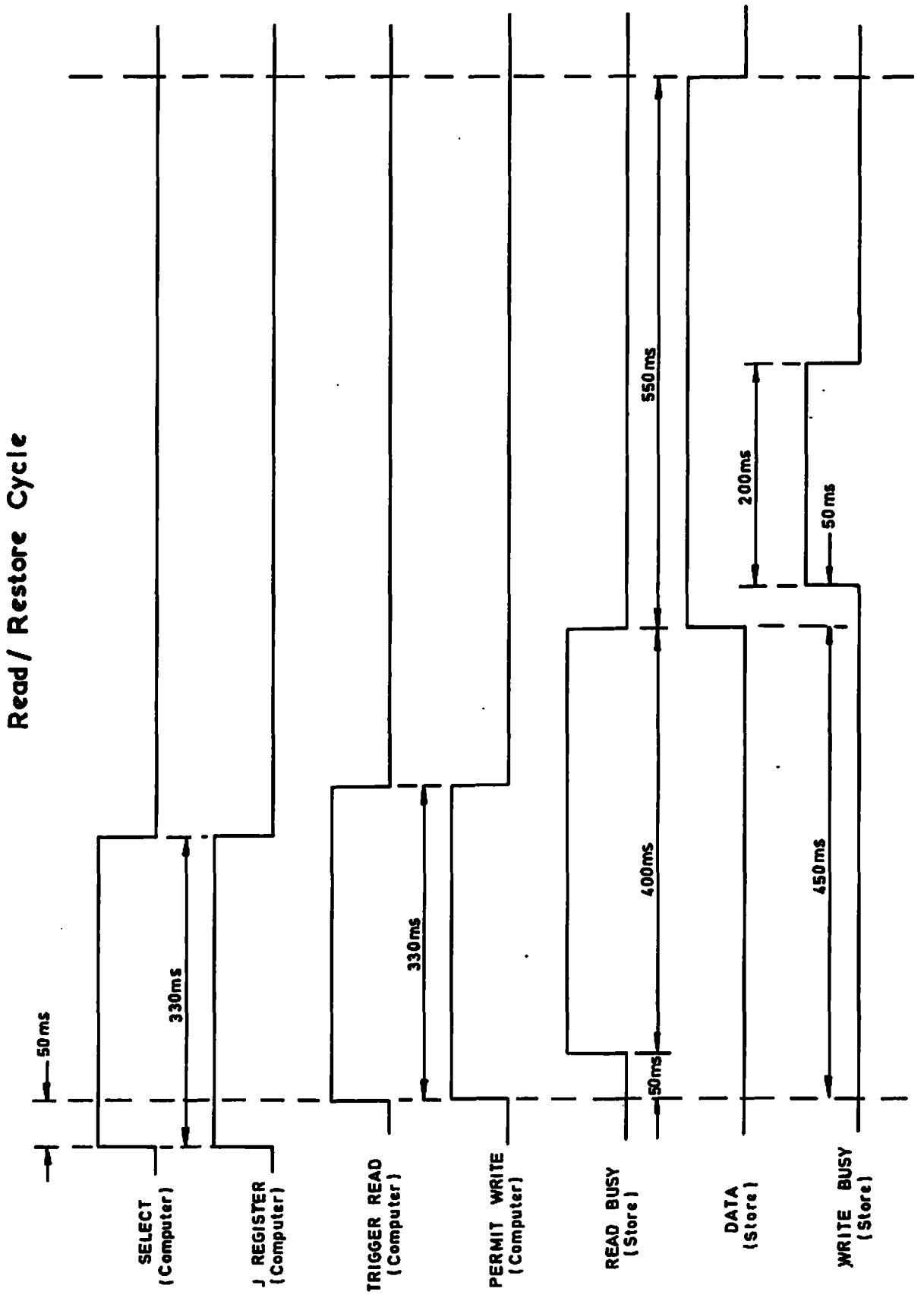
Block Input Timing

Fig. N° 3



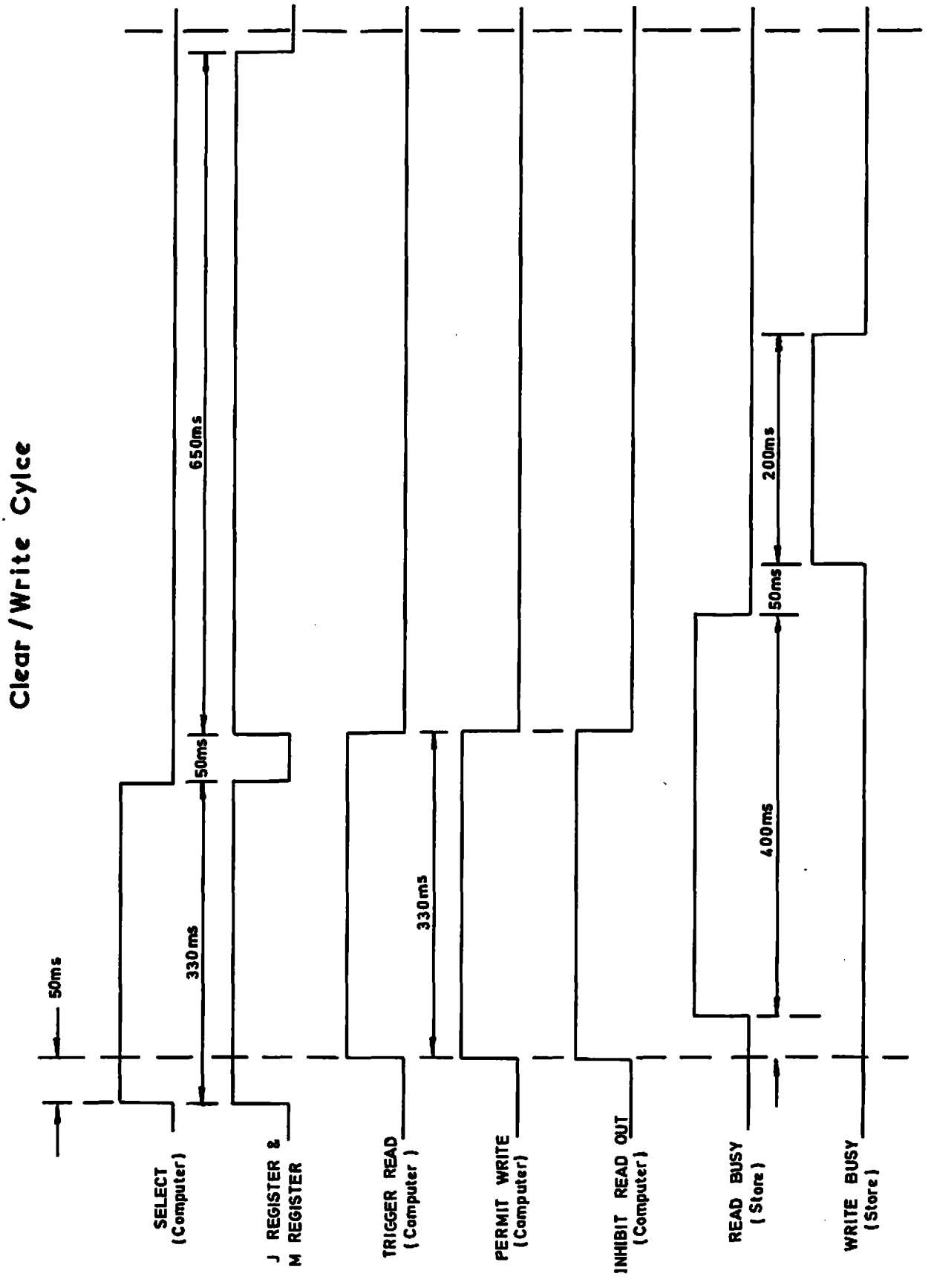
Block Output Timing

Fig. N°4



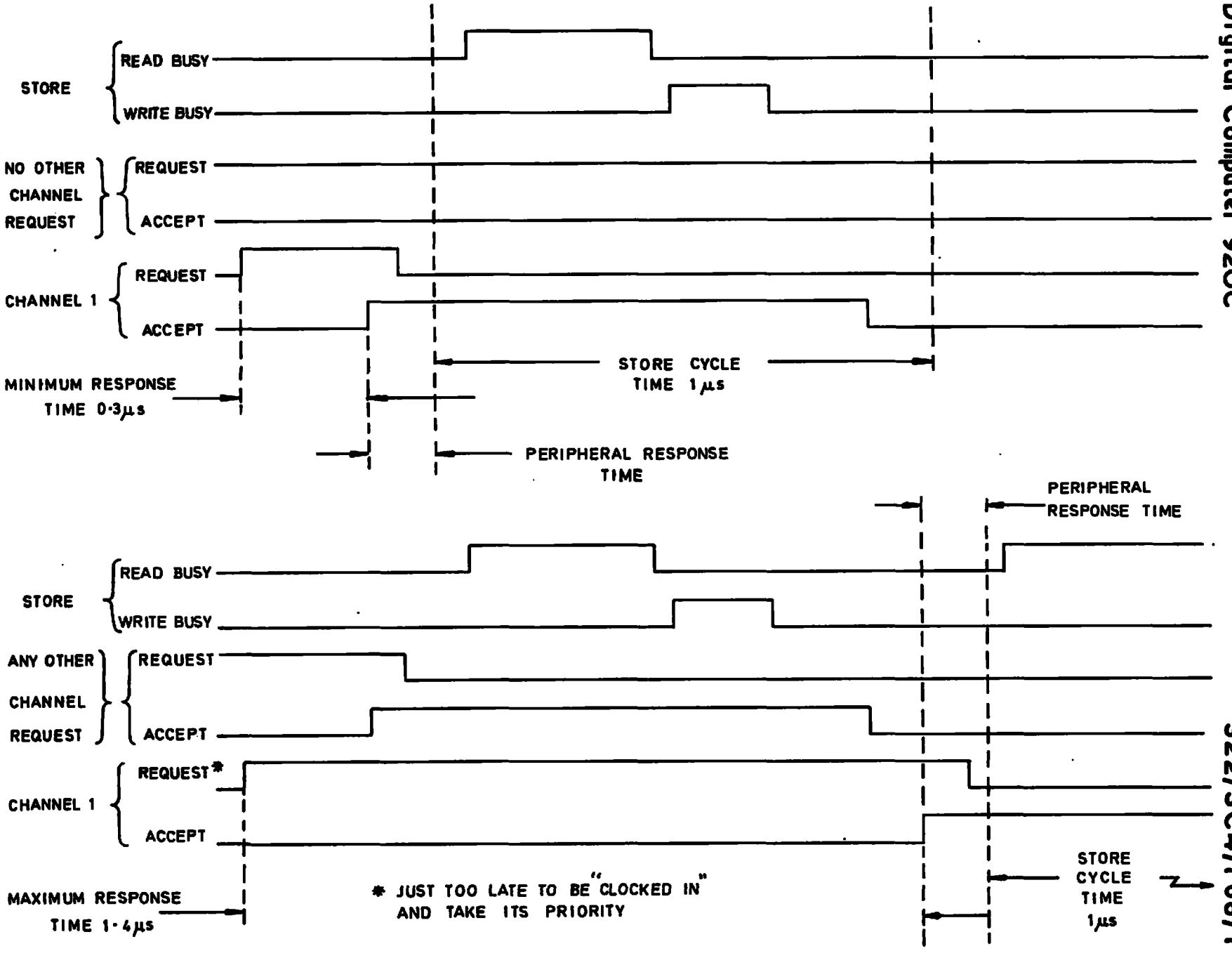
Data Input Timing

Fig. No 5



Data Output Timing

Fig. No 6

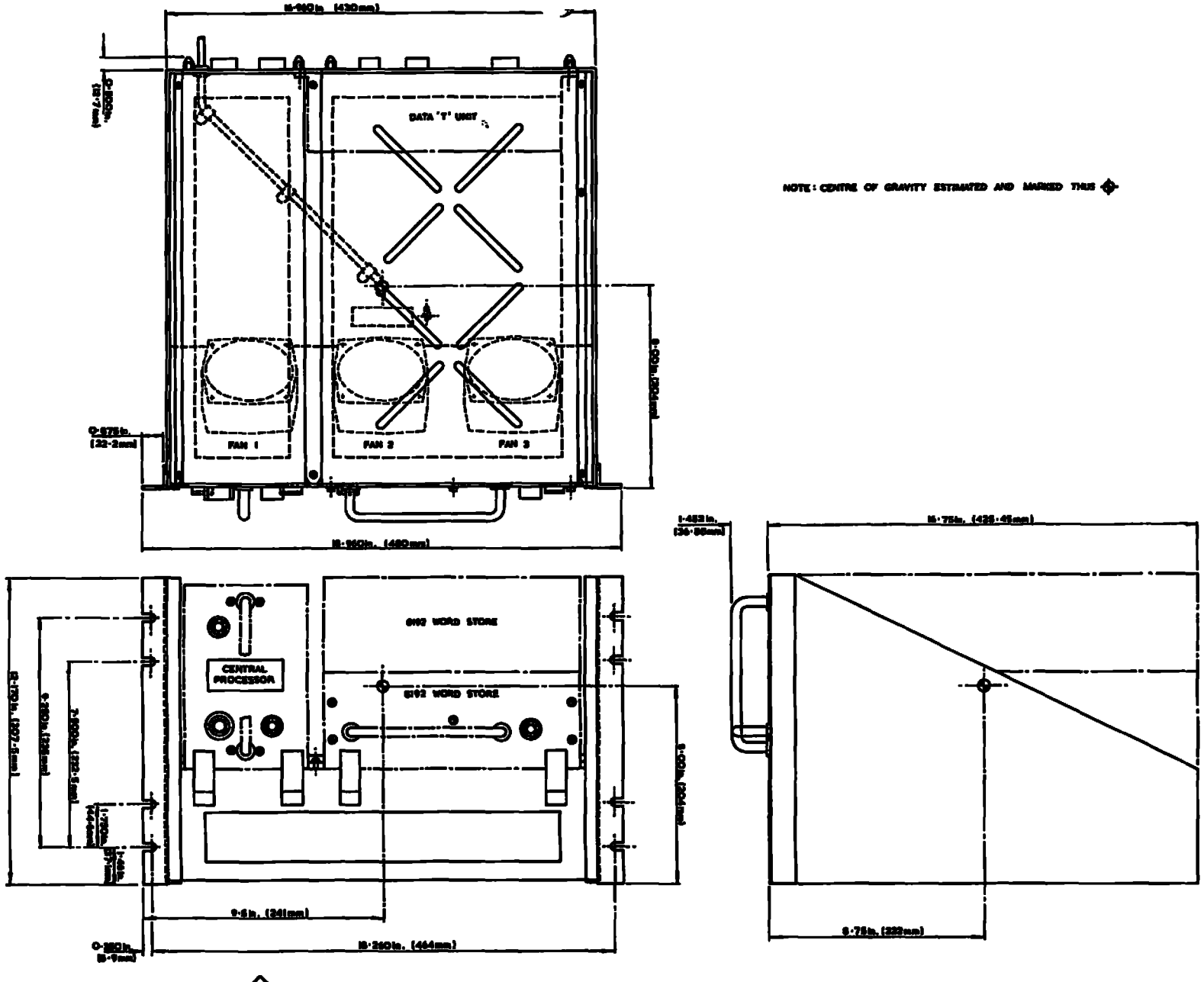


Digital Computer 920C

322/SC4/1·68/1

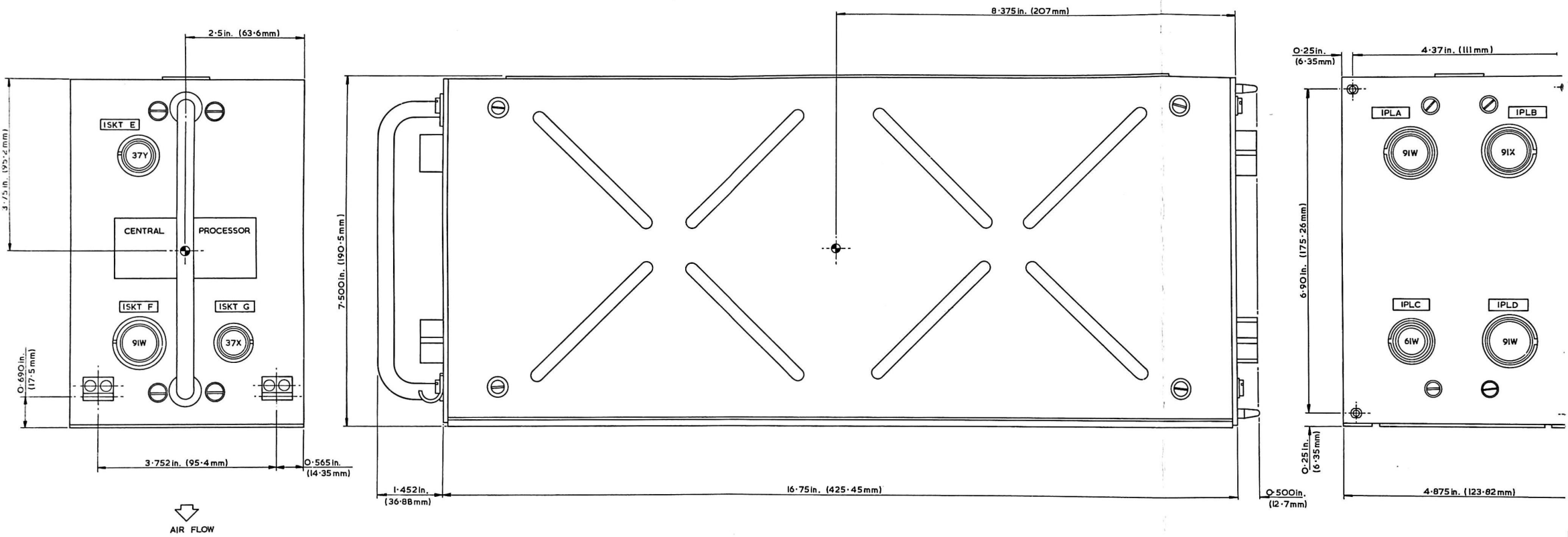
Autonomous Access Response Timing

Fig. No. 7



INSTALLATION DRAWING – 19 IN. CRADLE ASSEMBLY

MCS 920C COMPUTOR



ISKT E IS A HELLERMAN DEUTSCH CONNECTOR
37 WAY DSMOO 12-14-SY

ISKT F IS A HELLERMAN DEUTSCH CONNECTOR
91 WAY DSMOO 27-30-SW

ISKT G IS A HELLERMAN DEUTSCH CONNECTOR
37 WAY DSMOO 12-14-SX

IPLA IS A HELLERMAN DEUTSCH CONNECTOR
91 WAY DSMOO 27-30 PW

IPLB IS A HELLERMAN DEUTSCH CONNECTOR
91 WAY DSMOO 27-30 PX

IPLD IS A HELLERMAN DEUTSCH CONNECTOR
91 WAY DSMOO 27-30 PW

IPLC IS A HELLERMAN DEUTSCH CONNECTOR
61 WAY DSMOO 19-33 PW

INSTALLATION DRAWING — 920C CENTRAL PROCESSOR

SUPPLEMENT 'A'

TO SPECIFICATION MCC4

920C COMPUTER TEST FACILITY

1. INTRODUCTION

The compact construction of the 920C Computer has the effect of making normal servicing techniques inapt. In view of this fact, additional logic has been incorporated within the central processor which, in conjunction with a specialised tester, limits fault localisation to within a small number of replaceable logic modules, without opening the computer itself. The test unit is designed for use with any 920 computer, rendering the whole test process fully automatic, and enabling the experience of the design staff to be available to servicing personnel in the form of a computer program.

All the 900 series computers have facilities on their Control and Monitor units to enable the computer to be operated either one instruction at a time or one micro-instruction at a time, using data derived from the 18 bit word generator.

Monitoring lamps display the contents of the arithmetic registers and important control signals, thus allowing the progress of any desired instruction to be followed throughout the computer. With this information a service engineer can locate a fault to a replaceable unit.

However, the sequence of micro instructions within one instruction is not necessarily the best sequence for fault location, and for this reason additional logic is incorporated within the 920C to allow various control waveforms to be 'forced' by an external test unit. With the aid of these forcing waveforms more fundamental tests can be applied, allowing a standard sequence of operations for complete check-out of the processor. In all, 37 forcing waveforms can be applied to the 920C central processor, and the state of all registers and important control bistables can be monitored by gating the information onto a set of eighteen lines by one of eleven possible gating signals.

As more detailed control of the computer is made available, the servicing problem becomes less one of operator experience than one of data storage and retrieval, better handled by computer than by a large, if basically simple, maintenance manual. For this reason the test unit has been designed to allow another 920 computer to carry out the tests in a rapid and highly efficient manner.

2. TEST FACILITY COMPOSITION

2.1 Forcing Signals.

In the 920C the loop between the arithmetic register and the control section is broken logically. The control section includes

provision for a signal which inhibits normal operation by closing a set of gates, and further signals (forcing waveforms) from a test unit can define the operations required to take place. Reference should be made to Appendices 1 and 2.

The inhibiting signal ("Check") suppresses the action of the word sequence staticisor and the coded forcing signals ("Forcing Waveforms" 1 to 37) enter prescribed Fan In points in the Control Section. These coded signals thus simulate microprogram steps, resulting in the generation of normal waveforms, but under the selection of the operator.

A complete list relating the Forcing Waveform Code to the control waveform that is generated is given in Appendix 3. It should be noted that where the control waveform is "split" to cover two portions of the 18 bits (e. g. FTQ Bits 1 to 13 and FTQ Bits 14 to 18) the forcing waveform concerned (F. W. 18) forces both waveforms up together.

2. 2 Monitoring Waveforms

The outputs from the control and register sections are monitored, and include all the registers, important staticisors and most of the control waveforms. A total of 196 separate monitor waveforms are available, and in order to keep down the number of external connections a multiplex system has been adopted. The multiplexed output has 18 wires and allows a full 18 bit register to be monitored at a time, or a group of 18 control waveforms. Selection is obtained by coding the eleven select wires that feed into the central processor and provide the necessary gating signals for multiplexing. See Appendix 4.

The operator therefore, has available eleven different displays of 18 monitor outputs; 5 of these eleven selections will in turn, display the contents of the registers I, P, Q, A, S, J and M, and the states of two staticisors H and T. The remaining 6 selections will in turn, display the states of 85 control waveforms (including the 37 that can be forced) and 21 control staticisors.

A complete list of the monitor outputs that are available, and the coded input signals that are required, is given in Appendix 5.

3. FAULT LOCATION PROCEDURE

Assuming that a power supply unit and a test unit (as indicated in Appendix 2) are connected to the central processor under test, a standard sequence of operations can be performed by the operator, to test fully the arithmetic and control sections of the processor. Each step of the test sequence can be checked-out against the logic state of the monitor outputs.

When using the systematic check-out procedure, the fault area can be located to within 3 or 4 modules, and the final location of the faulty module will require direct monitoring of the back-wiring pins. Relatively few pins will need to be so monitored, once the faulty area has been established. An alternative to monitoring the back-wiring is to change all the modules in the fault area.

4. EXTENDED USE OF TEST UNIT

When the central processor has been checked-out satisfactorily, a store unit may be connected to the central processor and both units may be comprehensively checked-out together, under the control of the test unit.

This procedure may also be extended to include the peripherals.

5. THE 920C AUTOMATIC TESTER

5.1 Functional Specification

The tester is effectively an interface between the peripheral outlet of any 920 computer, (A, B, C, M) and all the outlets on a 920C central processor. This enables the testing computer to control and monitor all the signals going into and coming out of the central processor on test. The tester is built in D. T. L. micrologic Dual-in-line-packs on twelve $7\frac{3}{4}$" x 5" boards, the logic being arranged such that a single board, or a pair of boards, are associated with each connector on the central processor, which allows each outlet to be checked, and then connected to its particular unit, in any sequence and independent from the testing of the other outlets. For example, if the paper tape logic is found to be functioning correctly when connected to the tester, the actual paper tape equipment can be connected and checked, even though other outlets, e. g. the store outlet, are still connected to the tester.

The tester also connects with the power unit and can control the margins applied to any of the power rails. The power supply for the tester itself is built in. All the cables used to connect the tester to the central processor are the standard system cables, with the exception of the power cable, which must be connected via a short jumper cable to allow access by the tester to the forcing waveform input pins which are on the power connector.

In addition to testing the central processor, the unit can check out the store, although in order to do this at a realistic speed an additional unit, the store exerciser, is required. This unit is used during the factory commissioning of each store and tests the store at a very high speed in several worst case modes.

Since the tester controls the exerciser and the margins applied to the store, and during factory commissioning can sense the temperature at several points through the store unit, very thorough checking of each store can be undertaken, revealing relevant performance information for individual stores. This information can be used to detect deterioration in quality well before failure occurs.

All the interface circuits between the tester and the central processor or store under test are designed to present a worst case load to the circuit concerned, ensuring that the unit is not only capable of performing in its particular system, but can be readily interchanged with similar units in different systems.

5.2 Operation of the Tester.

The central processor and store to be tested are coupled to the tester and store exerciser respectively, all the standard system cables being used. The test program is read into the testing computer which then checks that the tester itself is serviceable and that all the necessary power supplies are available and within tolerance. The control section of the central processor is checked in detail, using all means of inputing information, i.e. program control unit, paper tape, store and peripheral connections, both by using the forcing waveforms and by performing the actual instructions in microprogram and complete form. The performance of the arithmetic unit is then checked by moving first specific and later random data words through the registers, again both by influence of the forcing waveforms and by the processor's own control circuits. The accuracy of the arithmetic operations performed on the data is checked by the testing processor acting on the same data itself, thus allowing completely random data to be used and enabling the use of data provided by local personnel should this denote a "worst pattern". If during any of these tests an error is detected, the symptons are stored within the testing computer, in terms of the waveforms concerned and the particular section which is failing. This information is used to qualify any further tests on this area of logic, enabling the testing to continue despite the presence of several simultaneous faults. At the end of the test sequence all the failing tests are output on paper tape, except where errors are attributable to the same fault, the correlation having been performed within the computer.

In the event of there being no errors the tests are repeated under progressively larger margins until either failure occurs or margin limits are reached. In the latter case it must be concluded that the fault lies outside the processor, is a function of the speed of operation of the machine, or is intermittent. However, since the machine is otherwise functioning correctly, a standard test program can be loaded from the testing computer via the processor under test into a serviceable store.

and the processor allowed to test itself at normal running speed. The testing computer is informed of the progress of each self-test cycle and varies the power margins in order to induce the fault.

The store can be tested at the same time as the central processor, the time sharing of the tester being completely at the discretion of the program; similarly any other automatic tester, capable of accepting information from the address and data busbar within the tester, can be controlled by the same 920. The paper tape control logic and the punch and reader may be tested individually or collectively by connecting them direct to the testing computer. If a 920B is being used to perform the testing operation, a short length of jumper cable will be required to provide mating connectors and to interchange 6V for 24V relay supply. The test tape is first loaded into the testing machine using equipment known to be serviceable, the units under test are connected and a standard data tape loaded into the reader. The program continues to test the equipment as far as is possible, giving an error output in a similar format to that for the computer.

The error output is initially in the form of a series of waveform names which together constitute the failing logical function. In order to relate these waveforms to a particular logic module a large amount of data representing the physical distribution of waveforms within the computer is required. Whether this data can be included in the test program depends on the size of store available on the testing computer and on the complexity of the test program. In any event the test program provided will depend on the ability of the servicing personnel, and should a highly sophisticated program be required to have a very detailed error output, together with some form of fault report, and have to be used with a 8 thousand word store, then two tapes are required, a fault location tape and data output tape. The latter is used in conjunction with the error output to give the required output format.

The tester is designed to check completely its own logic, which is of a basically simple form, and since integrated circuits are used throughout, is inherently reliable. There are approximately 150 integrated circuit packages within the tester, which is otherwise of similar construction to the 920B central processor, ensuring compatibility with a military environment. The test programs are punched on mylar tape to reduce wear and accidental damage.

6. CENTRAL PROCESSOR INTERFACE.

6.1 Signal Operating Details.

The central processor internal circuitry comprises integrated logic elements operating from a +5V level supply. The store and

peripheral interfaces incorporate transmitters and receivers designed for cable and (in the case of transmitters) multiple receiver loading.

The keyboard control and monitor unit interfaces consist of direct connection to the input terminals of the central processor logic elements, for incoming signals. Outgoing signals are generated directly from the output terminals of logic elements and connect to the interface via series protection resistors (150 ohms).

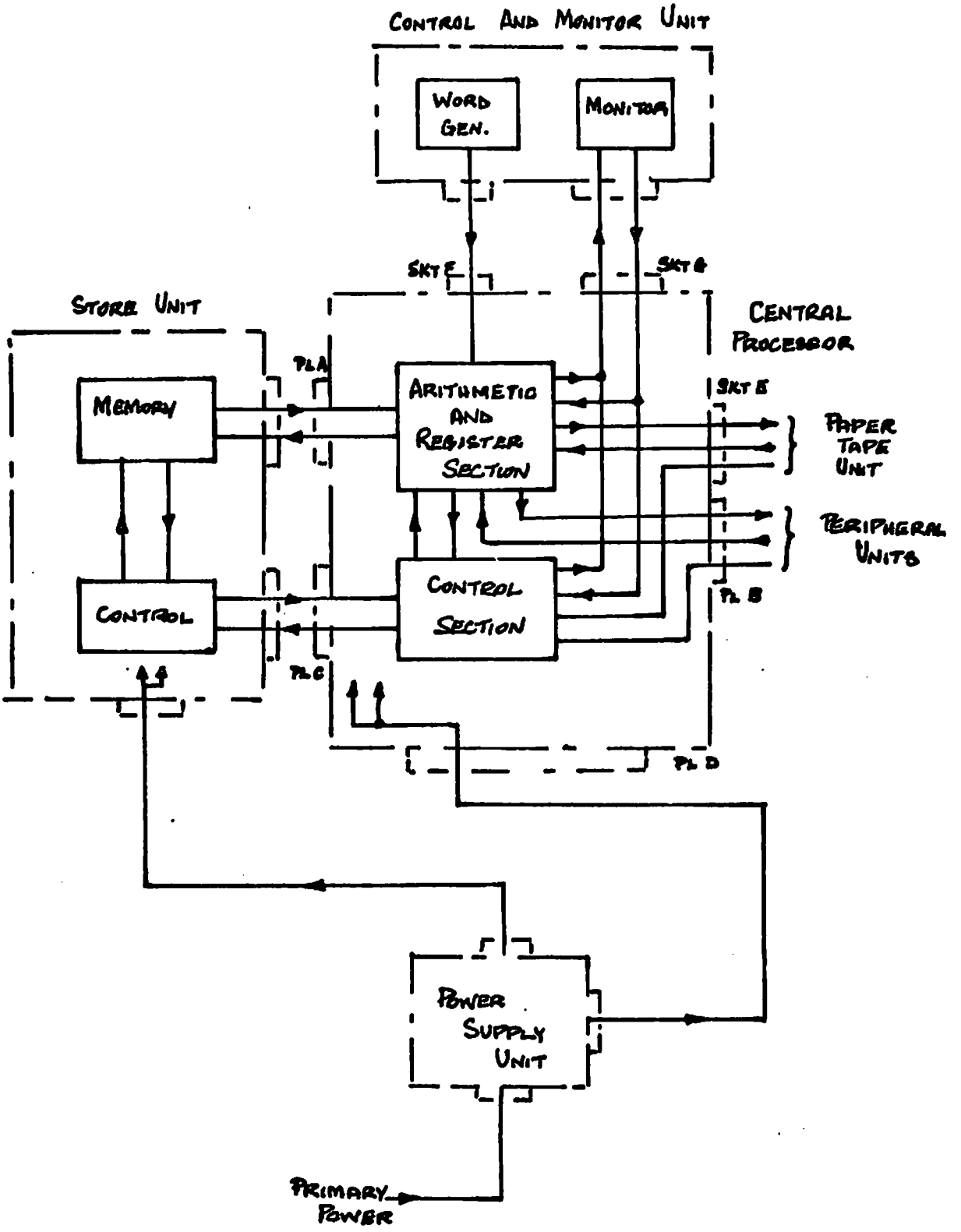
The incoming test forcing signals are on cables situated in the power supply interface, and make direct connection to the input terminals of logic elements in the control section of the central processor.

6.2 Interface Connection Details

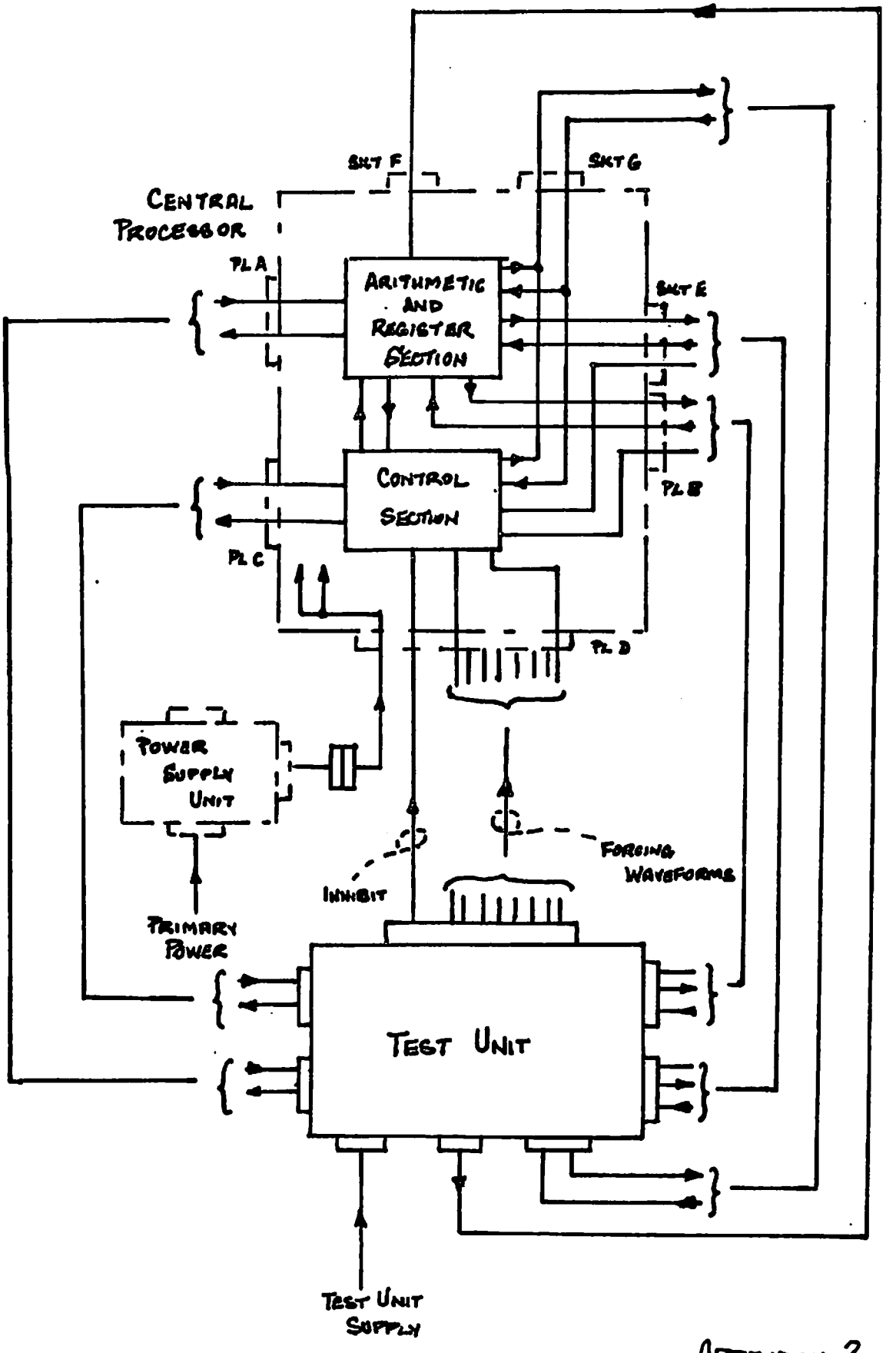
The interconnection details between the processor and the other system units are given in schedule form, in Specification 322/SC4/1.68/1. These schedules list the signal identity of each central processor connector pin.

7. LIST OF APPENDICES

Appendix No.	No. of Sheets	Detail
1	1	System Block Diagram
2	1	Test Block Diagram
3	1	Forcing Waveform Code
4		
5	1	Monitor Code and Display


CONTROL AND MONITOR UNIT
WORD GEN.
MONITOR
SKT F
SKT G
STORE UNIT
CENTRAL PROCESSOR
PL A
MEMORY
ARITHMETIC AND REGISTER SECTION
SKT E
PAPER TAPE UNIT
PERIPHERAL UNITS
CONTROL
CONTROL SECTION
PL B
PL C
PL D
POWER SUPPLY UNIT
PRIMARY POWER

APPENDIX 1

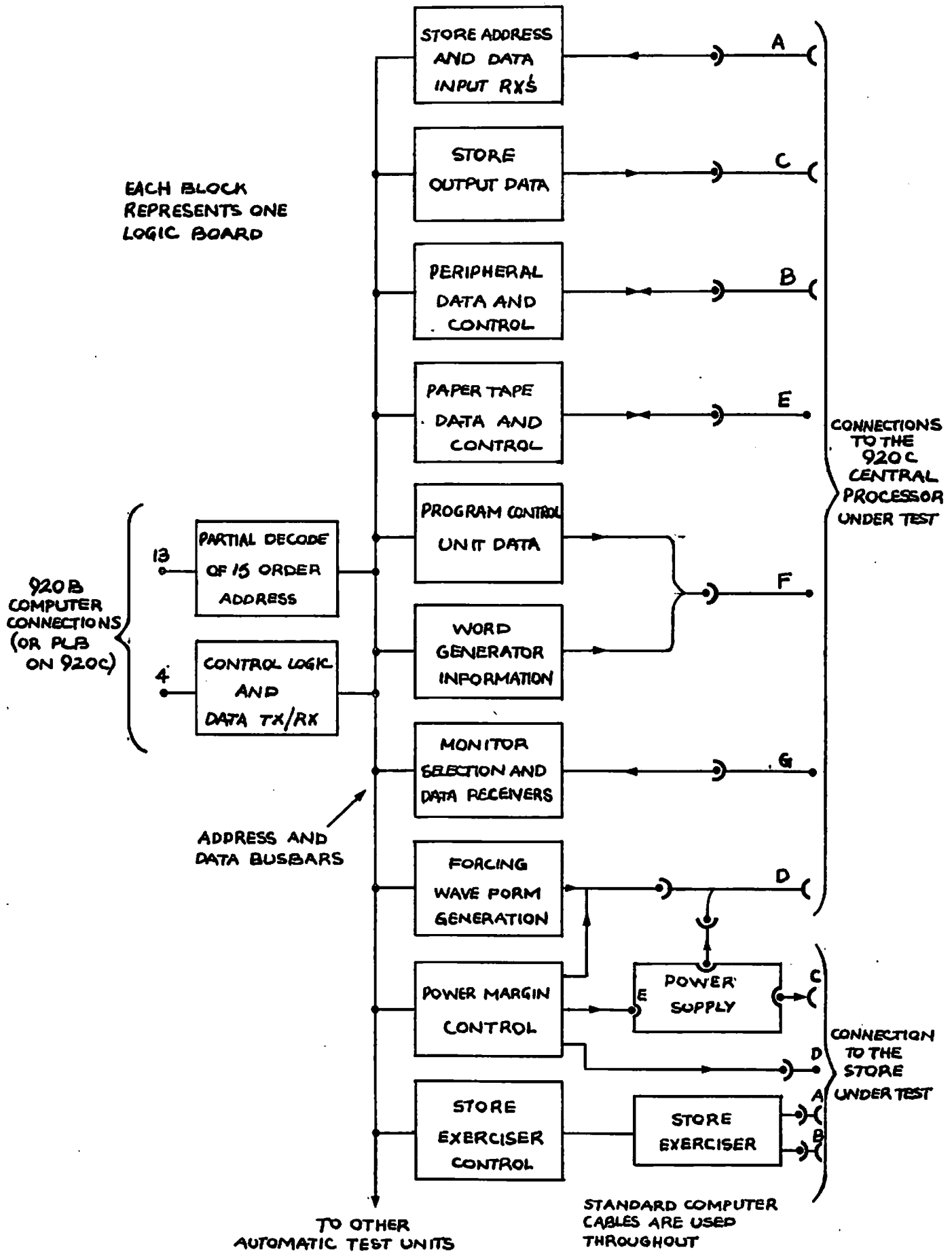

SKT F
SKT G
CENTRAL PROCESSOR
PL A
ARITHMETIC AND REGISTER SECTION
SKT E
CONTROL SECTION
PL B
PL C
PL D
POWER SUPPLY UNIT
FORCING WAVEFORMS
INHIBIT
PRIMARY POWER
TEST UNIT
TEST UNIT SUPPLY

APPENDIX 2

Forcing Waveform Code

In order to force any required processor control waveform, the input waveform "CHECK" must always be in the logic "1" state. Except when selected, all other Forcing Waveforms must be at logic "0" state.

Forcing Waveform Logic "1" state		Processor Control Waveform made active, i.e. Logic "1" state	
F.W. 1	F.W. 20	FTA	M,TR
2	21	LTA	IRO,TR
3	22	PTA1	QSR
4	23	PTA2	QS2R
5	24	RTA	FTS
6	25	2RTA	SITS
7	26	VTA	F18TT
8	27	1TF	ATX
9	28	FT1	$\overline{A}$TX
10	29	ETJ	QTX
11	30	FTJ	WTX
12	31	JITJ	MTY
13	32	SITJ	$\overline{M}$TY
14	33	K1-5	2MTY
15	34	QSL	$\overline{2}$MTY
16	35	FTM	JTY
17	36	MTP	STY
18	37	FTQ	SELH
19		SITMQ	



920C AUTOMATIC TESTER SCHEMATIC APPENDIX 4

Monitor Code and Display

Monitor Select Logic "1" State.	Monitor Outputs made active, i.e. Logic State is Displayed.																	
	Mon18	Mon17	Mon16	Mon15	Mon14	Mon13	Mon12	Mon11	Mon10	Mon 9	Mon 8	Mon 7	Mon 6	Mon 5	Mon 4	Mon 3	Mon 2	Mon 1
Mon A	A18	A17	A16	A15	A14	A13	A12	A11	A10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1
Mon Q	Q18	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10	Q 9	Q 8	Q 7	Q 6	Q 5	Q 4	Q 3	Q 2	Q 1
Mon P	Q0	I17	I16	I15	I14	P13	P12	P11	P10	P 9	P 8	P 7	P 6	P 5	P 4	P 3	P 2	P 1
Mon M	M18	M17	M16	M15	M14	M13	M12	M11	M10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1
Mon J	T	J17	J16	J15	J14	J13	J12	J11	J10	J 9	J 8	J 7	J 6	J 5	J 4	J 3	J 2	J 1
Mon S	H	S17	S16	S15	S14	S13	S12	S11	S10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
Mon T1	S0	S1	S2	S3	S4	S5	S6	S7	S 8	i0	I1	I2	NGO	-	TA	TB	-	MKR
Mon T2	ADT1	ADT2	ADT3	ADT4	ADT5	PTA2	PTA1	RTA	VTA	TRB	PR	TRI	RPT	2MTY	QTX	WTX	FTA	1TF
Mon C1	PROC	Z1	Z2	FTQM	QSR	FTS	2RTA	LTA	ETJ	FTM	EXT	FTI	STY	TR,M	ATX	$\bar{A}$TX	A=0	FTT
Mon C2	F20	F19	INT	QS2R	QSL	SITS	FTQL	SITJ	JITJ	SITMQ	TR,IRO	K1	JTYM	JTYL	MTYM	MTYL	RCP	$\bar{2}$MTY
Mon C3	SELTB	EWC	II	SELA	SELQ	SELS	SELJ	FTJL	SELH	SELM	SELI	FTJM	MTY	SELE	St Tm	MTP	NEXT	II Tm

Specification 322/SC3,4/Supp.B/5.68/1

SUPPLEMENT 'B'

TO SPECIFICATION MCC 3,4

RELIABILITY OF MCS 920C

CENTRAL PROCESSOR

*Supplement 'B' to Specification MCC 3, MCC 4.

RELIABILITY OF MCS 920C CENTRAL PROCESSOR

1. INTRODUCTION

There are two basic concepts which form the foundations for all procedures concerning the numerical reliability prediction for electronic equipments and systems. These two concepts stated simply are:-

(i) That equipments fail by performance degradation.

(ii) That in addition to performance degradation failures, equipments become inoperative because of random catastrophic failures of the parts (Ref.A.1)

Failures due to performance degradation are usually eliminated in modern equipment by good design, type testing and preventive maintenance. Reliability is therefore primarily determined by random catastrophic failures. Such failures are caused principally by thermal and electrical stresses, but under extreme environmental conditions mechanical stresses may be significant if the design of the equipment does not take care to minimise their impact.

Before discussing catastrophic failures, some of the measures taken to eliminate failures due to performance degradation will be described.

2. PERFORMANCE DEGRADATION FAILURES

A large proportion of the components in the 920C computer are employed in the logical circuits, and consequently the maximum design effort has been concentrated on ensuring their reliability.

It is essential in good design to strike a compromise between the use of the most modern components and techniques and the use of well-proved devices for which reliability statistics are available. The advantage of silicon integrated circuits and welding are so strong that both are used extensively in the 920C.

The integrated circuits are packaged in encapsulated modules; these are then clamped together and to the chassis forming an isothermal structure. Consequently a very low temperature gradient is attained. The thermal time constant of the complete unit is approximately 60 minutes and therefore short-term temperature variations can be ignored.

3. CATASTROPHIC FAILURES

3.1 M.T.B.F. - General

An accurate prediction of the mean time between failures (M.T.B.F.) of an equipment can only be made if reliable data regarding the failure rate of the component parts, in the appropriate environment, is available. In the case of a computer such as the 920C which uses modern components, particularly silicon integrated circuits and welding, it is inevitable that such data is not yet available. All that can be done therefore is to use the latest available information and the calculations which follow have been made on this basis. Even so, it is found that there is considerable divergence between the statistics for similar components from different sources, and it is necessary to study all the relevant factors carefully if a meaningful figure of M.T.B.F. is to be deduced.

Many of the relevant factors are not completely understood, and because of the low failure rates involved, it will be some years before reliable statistics can be produced. A study has been made of each class of component to deduce the most probable failure rate and this is summarised below. Failure rates are quoted as the percentage of the total population which may be expected to fail in a period of 1000 hours.

3.2 Silicon Integrated Circuits

There are 913 flat-pack integrated circuits in the Central Processor. Most are operated at less than 50% of their fan-out capability.

In the unit the integrated circuits are packaged in modular form, with up to 3 flat packs per module. Each module is mounted on a heat sink and encapsulated in epoxy resin.

Little information is available regarding reliability of integrated circuits. Different manufacturers and users assess and interpret 'failure rate' in quite individual ways.

As a basis for obtaining a reasonable failure rate, 'Microelectronics Survey' (Ref.E.6) and 'Reliability 65' (Ref.E.5) have been used. The former used data from 9 major vendors with total device hours of 700,000,000; the latter with device hours of 78,000,000. Ref. E6 shows a graph of failures against time from which is extracted the following:-

Failures 1964 - 0.12/million hours.

Failures 1965 - 0.012/million hours.

Ref.E.5 states a failure rate of 0.0012%/1000 hours in 1965.

From these reports it is confidently expected that the failure rate figure will decrease, and because this information is two years old it can be assumed that a failure rate lower than that shown could be adopted. Without more positive information therefore, the figure used for 920C is the Fairchild failure rate of 0.0012%/1000 hours.

3.3 Wrapped Joints

There are 9,400 wire-wrap joints in the central processor. To quote from G.W.A. Dummer (Ref.E.8):-

> "A wire is wrapped around a sharp-cornered metal post under conditions of controlled tension, using either a hand or power-operated tool. The actual contacts which occur at the corners of the sharp-edged post are gastight and, under test conditions, have resisted long periods of humidity cycling, repeated thermal shock, salt spray, etc.
> It is also claimed that the joints are less vulnerable to vibration damage than soldered connections".

"An airborne radar equipment employing wrapped and bound joints has achieved 144 million joint flying hours without failure".

"It appears from the evidence so far available that the wrapped joint has the lowest failure rate in operation of all known techniques. In a total of 6,750,000 joints, there has been only one recorded failure, and this was caused by a mechanically broken joint".

The failure rate adopted is 0.0001%/1000 hours.

3.4 Welded Joints

There are about 31,300 welded connections in the Central Processor. To quote G.W.A. Dummer (Ref.E.8):-

"Welding offers a very versatile and potentially reliable method of making connections. It is carried out under controlled conditions which eliminate most operator errors; the localised heat produced in the weld prevents damage to other heat-sensitive parts, and, because of the fusion of the materials, it posesses a high mechanical strength".

According to Dummer:

"Unfortunately, no British comparative figures on welded joints are yet available. Data from an American computer on 41296 welded joints over 825,870,000 joint hours give 30 failures; a failure rate of 0.00036% per 1000 hours".

Failure rates from different sources (Ref.E7 to E10) give figures for wrap joints as 0.0001%/1000 hours and ratios of weld/wrap varying between 5:1 and 0.715:1. Experience gained in use of the 920M computer leads us to believe that welding is not substantially worse than wrapping and hence a ratio of 2:1 can be expected, thereby making the failure rate for welded joints 0.0002% /1000 hours.

3.5 Soldered Joints

There are 460 soldered joints in the Central Processor. The latest information available is the S.R.D.E. report (Ref.E.7), which gives a failure rate of 0.0005%/1000 hours. Experience in the use of the 920B computer, with an expected failure rate of 0.0007%/1000 hours, indicates that the predicted rate is not optimistic. Hence the figure adopted for the 920C is 0.0005%/1000 hours.

3.6 Transistors

There are 46 single and 11 dual silicon planar transistors in the central processor. According to Fairchild (Ref.E.5):-

> "In extended operating life tests on a typical device in connection with the Minuteman program a total of 84.6 million transistor-hours generated a failure rate of 0.002%/1000 hours".

Experience with the 920B computer indicates a M.T.B.F. in use in excess of that predicted. As so little information is available regarding these devices the figures used for this unit are 0.01%/1000 hours for single transistors and 0.002%/1000 hours for dual transistors.

3.7 Diodes

There are 72 silicon planar diodes in the 920C Central Processor. A failure rate of 0.0025% was used to predict the M.T.B.F. of the 920B computer and experience has shown this to be pessimistic.

Fairchild (Ref.E.5) quote 0.00001%: as these figures are widely divergent, an intermediate value of 0.001%/1000 hours has been used for the 920C Central Processor.

3.8 Resistors

3.8.1 Resistors (Fixed)

There are 819 resistors in the unit of the metal oxide film type, mainly Welwyn type F25 or Electrosil TR4(NJ65).

In the 920B Reliability Report a figure of 0.001%/1000 hours was obtained for resistors of the same types and this figure is again used for this unit.

3.8.2 Resistors (Variable)

There are 18 wire-wound variable resistors used in 920C, all Painton-Bourne "Trimpots".

Reference E9, (E.F.A. Report) gives a ratio variable/fixed of 16:1 hence the figure used is 0.016%/1000 hours.

3.9 Capacitors

There are 76 capacitors of the solid tantalum (polar) type and 19 glass types. Study of various reports (Ref.E7 to E10) gives a ratio of tantalum/glass varying from 2:1 to 4:1. Experience has indicated a ratio of 2:1 and a failure rate of 0.0017/1000 hours for glass. The rate for tantalum thus becomes 0.0034%/1000 hrs.

3.10 Connectors

The unit has 460 active pins using Hellerman-Deutsch connectors to external equipment.

Ref.A.7. is the only source which is sufficiently explicit to be reliable. A worst case assumption for failure rate per pin would be 0.001%/1000 hours.

3.11 Crimped Joints

There are 460 crimped connections in the unit and all are used in the Hellerman-Deutsch connectors.

A failure rate figure from the E.F.A. Report (Ref.E9) quotes 0.001%/1000 hours.

4. M.T.B.F. of MCS 920C COMPUTER

Component	Qty	Failure Rate %/1000 Hours	Failure Rate No./1000 Hours
Resistors (fixed)	819	0.001	0.00819
Resistors(variable)	18	0.016	0.00288
Capacitors (Tantalum)	76	0.0034	0.00258
" (Glass)	19	0.0017	0.00032
Transistors, single	46	0.002	0.00092
Transistors, dual	11	0.002	0.00022
Diodes	72	0.001	0.00072
Integrated Circuits	913	0.0012	0.01096
Welded Joints	31,320	0.0002	0.06264
Wrapped Joints	9,348	0.0001	0.00935
Soldered Joints	460	0.0005	0.00230
Crimped Joints	460	0.001	0.00460
Pin Connections	460	0.001	0.00460
			0.11028

The M.T.B.F. on the basis of these statistics is therefore:-

$$\frac{1000}{0.11} = 9090 \text{ hours.}$$

Many of the substantial advances in component reliability of the last few years have still to be reflected in equipment performance, but targets of 10,000 hours for M.T.B.F. are by no means unrealistic. (Ref.B.2,A. 4). It is thus considered that the figure quoted is reasonable in relation to past experience and future expectations. Since the 920C uses only components with the highest expectations of reliability the figure quoted could be substantially exceeded.

The effect of environment is important. This can

affect the M.T.B.F. of equipments by as much as a factor of 100. (Ref. C.3). However, it must be remembered that such factors result from an increase in the thermal and mechanical stresses that are applied to components. Such factors are minimised in this computer because of its ruggedised construction. Thermal stress is limited by the fact that all components are mounted on heat sinks and that the computer itself is so constructed as to act as a very large heat sink.

Tests for vibration up to 5G have been conducted without ill-effect and, because the modules and backwiring are encapsulated, contamination, moisture and corrosive substances are excluded.

Experience with the 920B and 920M computers shows that the predicted M.T.B.F. may well be exceeded.

5. CONCLUSIONS

Based on the statistical data and assumptions stated above the M.T.B.F. of the 920C Central Processor is expected to be not less than 9000 hours.

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2. As above. p.408. Table 1.

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7. Components Circular No. 35. S.R.D.E. 1967.

8. Electronic-circuit Connections. G.W.A. Dummer. 1966.

9. 1966 Handbook for Reliability Prediction. Elliott Flight Automation.

10. Electronic Equipment Reliability Assessment. Electronic Components Supplement - September 1967. G.W.A. Dummer.

SPECIFICATION

MCS 920C MEMORY UNIT, 1 μs, 8192 Words.

Catalogue No. MCC 14

1. GENERAL DESCRIPTION

This specification refers to a random access, coincident current, magnetic core memory system having a cycle time of 1 μs and an access time better than 450 ns.

Each unit has 8192 addressable locations of 18 bits, and a system can be built up using multiples of 8192 word blocks, up to a maximum of 65,536 words.

Each unit incorporates a parity check facility, an external indication being given when a parity error occurs.

Parts of the store may be protected against over-writing. This facility "locks out" blocks of 1024 words in the store, the location of the block being controlled externally.

2. TECHNICAL SPECIFICATION

Modes of Operation:	Read/Restore Clear/Write Read-Modify-Write
Input Signal Lines:	Trigger Read Permit Write Inhibit Read Output Store Select (a separate signal is required for each store unit) 18 Data Input (address and data information are multiplexed on the same lines) Lock Out Interlock Initial Reset
Output Signal Lines:	Read Busy Write Busy 18 Data Output Parity Error Lock Out Error Interlock

2.1 Electrical Characteristics of Interface:

All signals to and from the store shall be sent via twisted pair cables of characteristic impedance 120 ohms which are terminated at each end with 120 ohms to OV.

2.2 Power Requirements

The power supply requirements for an 8192-word 18-bit store unit are as follows:

1. + V1 (28V fixed) 1.75A
2. + V2 (30V variable) 3A
3. + 6V (floating on V1) 1.25A
4. + 5V 4.5A
5. -6V 0.5A

These are the power supply requirements for one store unit. Where more than one store is connected to the same power supply the additional requirements per store are as follows:

1. +V1 (28V fixed) 0.75A
2. +V2 (30V variable) - NIL
3. +6V (floating on V1) 1.25A
4. +5V 4.5A
5. -6V 0.5A

The average power dissipation of one 8192-word unit is 110 watts, the maximum being 150 watts.

The power supplies shall be sequenced so that Supplies 1, 4 and 5 come on instantaneously in response to the ON signal, followed by Supplies 2 and 3 after a period of not less than 2 ms. The switch-off sequence shall be in the reverse order.

3. EXTERNAL INTERFACE SIGNALS.

The store timing is asynchronous with respect to any external system, the control and timing being performed by the following signals. All timings are referred to the interface between the store circuits and the cable connecting it to the system.

3.1 Signals to the Store

3.1.1 Store Select

A logic "1" allows the selected unit to respond to the control signals. The level must be established 50 ns. before the start of Trigger Read, and must remain for a minimum period of 100 ns.

3.1.2 Trigger Read

A logic "1" pulse will initiate the cycle of the selected unit. The Trigger Read pulse must have a minimum duration of 100 ns.

3.1.3 Permit Write

A logic "1" pulse will allow the write part of the store cycle to occur. The timing of the Permit Write signal will determine the type of cycle to be performed by the Store. The Permit Write pulse must have a minimum duration of 100 ns.

3.1.4 Inhibit Read Output

A logic "1" allows a Clear/Write cycle to occur. The level must be established not later than 100 ns. after the leading edge of Trigger Read, and must remain for a minimum period of 100 ns.

3.1.5 Data Input

The Data Input lines are multiplexed, carrying both address and data information. The store requires 18 data input lines carrying information in the true phase. 13 of these lines will carry the address information.

The address information shall be established not later than 50 ns. before the start of Trigger Read and shall remain until 200 ns. after the start of Trigger Read.

The input data shall be established not later than 350 ns. after the start of Trigger Read, or not later than 50 ns. before the leading edge of Permit Write, whichever is later. The input data shall remain established until 200 ns. after Write Busy has gone to the logic "1" level.

3.1.6 Lock Out

A logic "O" level will cause the Store to perform Read/Restore cycles on selected locations regardless of the timing of Permit Write and Inhibit Read Output. These locations are in

blocks of 1024 words and selection of the block is performed externally. There are 8 blocks of 1024 words and any combination of these blocks can be selected via the monitor socket on the front of each store unit by connecting the selected line to the logic "1" level.

3.1.7 Store Reset

A reset signal must be provided to ensure that all bistables within the store are held in the reset state during the switching sequence of the power supplies.

Switch On: Store Reset shall be held in the logic 'O' state and remain in this state until all supplies have been established. After this time Store Reset shall go to the Logic '1' level, and the store can then be accessed.

Switch Off: Store Reset shall return to the logic 'O' level not later than 10 µs. after the switch off sequence has been initiated.

Power Supply Failure: Store Reset shall return to the logic 'O' level not later than 10 µs. after the Interlock signal has gone to the logic 'O' level.

3.2 Signals from the Store

3.2.1 Read Busy

Read Busy will go to the logic '1' level not later than 50ns. after the leading edge of Trigger Read, and will return to the logic 'O' level at the end of the Read Cycle, which will be not later than 500 ns. after the leading edge of Trigger Read.

3.2.2 Write Busy

Write Busy will go to the logic '1' level not later than 50 ns. after Read Busy has gone to the logic 'O' level, or not later than 100 ns. after the leading edge of Permit Write, whichever is later. The end of the Write Busy signal is adjustable from 0 to 300 ns. before the end of the store cycle, so that the end of the cycle can be anticipated to allow for cable delays.

3.2.3 Data Output

There are 18 Data Output lines giving true phase output signals. The appearance of the information on the data output lines will occur not later than 450 ns. after the leading edge of Trigger Read. The data output information will remain

established until the data input information is set into the register. When no data input information is sent to the store (Read/Restore cycle) the data output information will remain established until the end of the cycle.

3.2.4 Parity Error

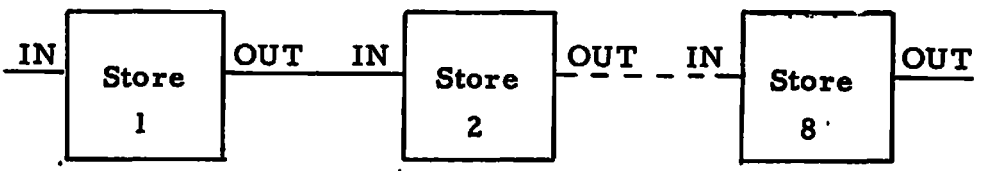
A parity unit may be included within the store to check the parity of the data information. If the parity is not correct a logic '1' signal will be given not later than 150 ns. after the data output information. The signal will remain in the logic '1' state until the end of the cycle.

3.2.5 Lock Out Error

If a 'locked out' location of the store is addressed in any other mode than Read/Restore, a logic '1' level will be established on this line. The logic '1' level will be established not later than 100 ns. after the start of the erroneous signal and shall remain in the logic '1' state until the end of the cycle.

3.3 Interlock

The interlock system is shown below:



Any unit which goes out of limits (voltage or temperature) will give a logic 'O' level at Interlock Out, thus causing a logic 'O' level at all subsequent points. Interlock In for Store 1 must be connected to the logic '1' level.

3.3.1 In Limits

'In limits' for each store unit can be monitored via the front socket. A logic 'O' level indicates the unit is within limits. This signal will be able to drive a low power indicator lamp. (150mA maximum current).

3.4 Modes of Operation

The modes of operation are determined by the timing of Permit Write and Inhibit Read Output.

3.4.1 Read/Restore Cycle

Permit Write shall go to the logic '1' state not later than 250 ns. after the leading edge of Trigger Read.

Immediately after the completion of the read half cycle, the store performs a write half cycle to write the read out data back into the same location of the store.

3.4.2 Read-Modify-Write Cycle

Permit Write shall not go to the logic '1' state until after Read Busy returns to the logic 'O' state.

On completion of the read half cycle, the store waits until Permit Write initiates the write half cycle to write new data into the addressed location.

3.4.3 Clear/Write Cycle

Inhibit Read Output shall go to the logic '1' state not later than 100 ns. after Trigger Read.

The store is cleared during the read half cycle, and the contents of the data register will be zero. New information is written into the addressed location during the write half cycle.

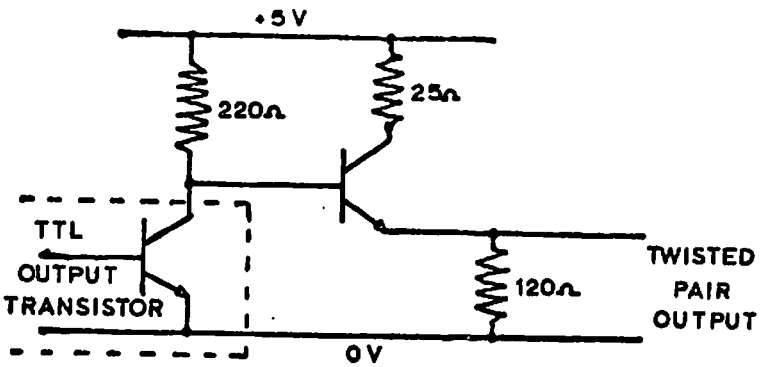
3.5 Interface Circuits

3.5.1 Transmitter

The logic output levels of the transmitter are as follows:-

Logic 'O' is 0.5v maxm.
Logic '1' is 2.8v minm.

The output circuit of the transmitter is shown below:

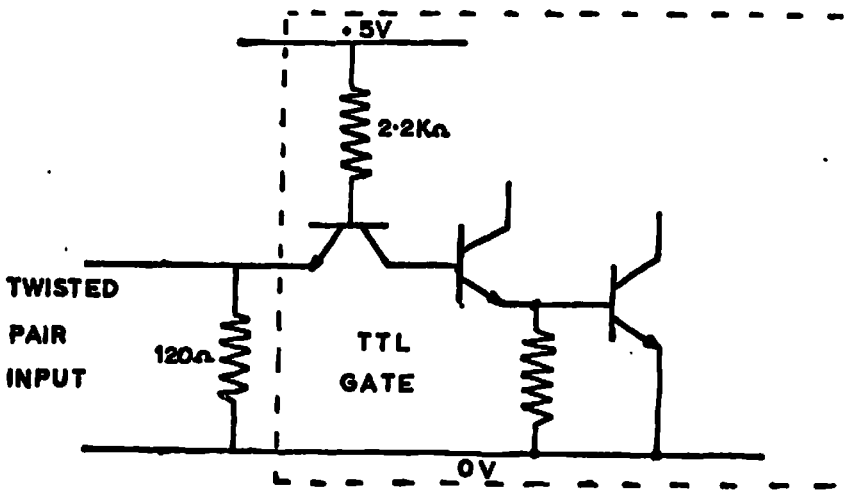


3.5.2 Receiver

The input threshold levels of the receiver are as follows:-

Logic '1' is 1.8v minm.
Logic 'O' is 0.8v maxm.

The input circuit of the receiver is shown below:



The receiver is a T^2L gate having 120 ohms connected between the input and 0V.

3.6 Timing

The timing diagrams for the three modes of operation are shown in Figs. 2-4. The cycle time for a Read/Restore Cycle and a Clear/Write Cycle will be 1.0 μs. and the timing for a Read-Modify-Write Cycle will be 1.10 μs. + T. (T is the waiting time between the read half cycle and the write half cycle and shall be not less than 50 ns.).

4. ENVIRONMENTAL SPECIFICATION

4.1 General

The 920C Memory Unit (MCC14) has been designed to be suitable for most service applications. In general the design is based on specification DEF-133 Class L.2, covering Ground Equipment - Partially Protected; and Class A2, covering Airborne Equipment - High Flying.

4.2 Equipment Characteristics.

4.2.1 Operating Temperature.

The unit will operate within specification over an ambient temperature range of 0°C to + 70°C.

4.2.2 Cooling

The unit requires an external supply of cooling air, of 3.5 lbs/minute mass flow.

4.2.3 Method of Mounting

The unit may be mounted in any attitude.

Note: The most preferable attitude (when functioning) is with cooling air passing vertically through the unit.

4.2.4 Finish

The external surface of the equipment is paint finished to specification DEF-1059, colour matt black.

4.2.5 Radio Interference

The unit is not vulnerable to Radio Interference when installed with the Power Supply Units supplied by Mobile Computing Division. (In these power supply units the power lines are suppressed to above 70dB over the range 50Kc/s to 1,000 Mc/s and above 40dB over the range 10Kc/s to 50Kc/s). All relevant inter-connecting cables supplied are screened to minimise radiated interference.

4.3 Design Standard

The equipment is designed to meet the following tests:-

	Test	DEF 133 Clause
(i)	Visual Examination	6.1.
(ii)	Resonance Search To figure 7, curve D. The unit will be required to function satisfactorily during test	8.1. (A)
(iii)	Vibration Function To figure 7, curve D. The unit will be required to function satisfactorily during test.	8.2.

	Test	DEF 133 Clause
(iv)	Vibration Endurance To figure 7, curve D. Tests C and G2. The unit will be required to function satisfactorily during test.	8.3 (C & G2)
(v)	Acceleration Proof acceleration : 6.5g; the unit will be required to function satisfactorily after end of test.	9.1.
(vi)	Acceleration The unit will not be required to function after end of test.	9.2.
(vii)	High Temperature/Low Pressure Temperature of +55°C and a pressure of 280mm Hg for 16 hours. Perform function test to DEF 133.	12.3.
(viii)	Low Temperature Exposure The unit will not be required to function after end of test.	12.1.(B)
(ix)	Dry Heat Excluding measurement of surface temperatures. The unit will be required to function satisfactorily during test.	11.0 (A)
*(x)	Low Temperature/Low Pressure Increase temperature until chamber and unit stabilise at -10°C when the unit will be required to function.	12.2.(B)
*(xi)	Damp Heat Perform function test to DEF 133.	11.1.
(xii)	Tropical Life Test Function unit after 14 and 28 days.	11.2.
(xiii)	Mould Growth To be carried out on representative samples.	11.3. * 4 cycles.

Test	DEF 133 Clause
(xiv) Corrosion Test Connector covers or cables to be fitted. The unit will be required to function satisfactorily after end of test.	14.0. 14.1. 14.2.
(xv) Contamination Test Carry out function test after end of test.	14.3.
(xvi) Dust and Sand Connector covers fitted. Presence of dust or sand shall not affect functional performance,	10.0.
(xvii) Drop Test The unit shall be dropped from 1 inch onto each corner and end faces. The unit will be required to function satisfactorily after end of test.	7.1.
(xviii) Toppling test The unit shall stand on either of narrowest face and be toppled 3 times onto either of its broadest face. Test shall be carried out without covers fitted. The unit will be required to function satisfactorily after end of test.	7.4.
(xix) Bump Test Test A. The unit will be required to function satisfactorily after end of test.	7.0 (A)

5. MECHANICAL CONSTRUCTION

Configuration (See Fig. 1.)

Single unit, 8192 words.	Double unit, 16,384 words.
Length : $16\frac{3}{4}$" (425mm)	$19\frac{1}{2}$" (495mm)
Width : 10.1/8" (258mm)	10.1/8" (258mm)
Height : 3.9" (99.5mm)	7.1/8" (181mm)
Weight : 30 lb (approx) (13.63 Kg)	60 lb (approx) (27.4 Kg)

6. INTERCONNECTIONS

Plug 2 PLA - Store Unit to Central Processor (DS MOO 27-30 PL)

Pin No.	Signal Name.	
1	ITS BIT 1	Twisted pairs
2	Earth	
3	ITS BIT 2	Twisted pairs
4	Earth	
5	ITS BIT 3	Twisted pairs
6	Earth	
7	ITS BIT 4	Twisted pairs
8	Earth	
9	ITS BIT 5	Twisted pairs
10	Earth	
11	ITS BIT 6	Twisted pairs
12	Earth	
13	ITS BIT 7	Twisted pairs
14	Earth	
15	ITS BIT 8	Twisted pairs
16	Earth	
17	ITS BIT 9	Twisted pairs
18	Earth	
19	ITS BIT 10	Twisted pairs
20	Earth	
21	ITS BIT 11	Twisted pairs
22	Earth	
23	ITS BIT 12	Twisted pairs
24	Earth	
25	ITS BIT 13	Twisted pairs
26	Earth	
27	ITS BIT 14	Twisted pairs
28	Earth	
29	ITS BIT 15	Twisted pairs
30	Earth	
31	ITS BIT 16	Twisted pairs
32	Earth	
33	ITS BIT 17	Twisted pairs
34	Earth	

Pin No.	Signal Name.	
35	ITS BIT 18)	Twisted pairs
36	Earth)	
37	Spare	
38	Spare	
39	Spare	
40	Spare	
41	Spare	
42	Spare	
43	Spare	
44	Spare	
45	Spare	
46	Spare	
47	Spare	
48	Spare	
49	Spare	
50	Spare	
51	Trigger Read)	Twisted pairs
52	Earth)	
53	Permit Write)	Twisted pairs
54	Earth)	
55	Inhibit Read Out)	Twisted pairs
56	Earth)	
57	$\overline{\text{Store Reset}}$)	Twisted pairs
58	Earth)	
59	Interlock)	Twisted pairs
60	Earth)	
61	$\overline{\text{Lock Out}}$)	Twisted pairs
62	Earth)	
63	Store Select 1)	Twisted pairs
64	Earth)	
65	Store Select 2)	Twisted pairs
66	Earth)	
67	Store Select 3)	Twisted pairs
68	Earth)	
69	Store Select 4)	Twisted pairs
70	Earth)	
71	Store Select 5)	Twisted pairs
72	Earth)	

Pin No.	Signal Name	
73	Store Select 6)	Twisted pairs
74	Earth)	
75	Store Select 7)	Twisted pairs
76	Earth)	
77	Store Select 8)	Twisted pairs
78	Earth)	
79	Spare	
80	Spare	
81	Spare	
82	Spare	
83	Spare	
84	Spare	
85	Spare	
86	Spare	
87	Spare	
88	Spare	
89	Spare	
90	Spare	
91	O volts.	Screen

Plug 2 PLB Store Unit to Central Processor (DSMOO19-33 PW)

Pin No.	Signal Name	
1	DFS BIT 1)	Twisted pairs
2	Earth)	
3	DFS BIT 2)	Twisted pairs
4	Earth)	
5	DFS BIT 3)	Twisted pairs
6	Earth)	
7	DFS BIT 4)	Twisted pairs
8	Earth)	
9	DFS BIT 5)	Twisted pairs
10	Earth)	
11	DFS BIT 6)	Twisted pairs
12	Earth)	
13	DFS BIT 7)	Twisted pairs
14	Earth)	

Pin No.	Signal Name	
15	DFS BIT 8	Twisted pairs
16	Earth	
17	DFS BIT 9	Twisted pairs
18	Earth	
19	DFS BIT 10	Twisted pairs
20	Earth	
21	DFS BIT 11	Twisted pairs
22	Earth	
23	DFS BIT 12	Twisted pairs
24	Earth	
25	DFS BIT 13	Twisted pairs
26	Earth	
27	DFS BIT 14	Twisted pairs
28	Earth	
29	DFS BIT 15	Twisted pairs
30	Earth	
31	DFS BIT 16	Twisted pairs
32	Earth	
33	DFS BIT 17	Twisted pairs
34	Earth	
35	DFS BIT 18	Twisted pairs
36	Earth	
37	Spare	
38	Spare	
39	Spare	
40	Spare	
41	Spare	
42	Spare	
43	Spare	
44	Spare	
45	Spare	
46	Spare	
47	Spare	
48	Spare	
49	Spare	
50	Spare	
51	Read Busy	Twisted pairs
52	Earth	

Pin No.	Signal Name	
53	Write Busy)	Twisted pairs
54	Earth)	
55	Interlock)	Twisted pairs
56	Earth)	
57	Parity Error)	Twisted pairs
58	Earth)	
59	Lock Out Error)	Twisted pairs
60	Earth)	
61	O volts	Screen

Plug 2 PLC StoreUnit to Power Supply. (DSMOO 12-14 PX)

Pin No.	Signal Name
1	+ 5 volts
2	+ 5 volts
3	+ 5 volts
4	+ 5 volts
5	+ 5 volts
6	0 volts
7	0 volts
8	0 volts
9	0 volts
10	0 volts
11	0 volts
12	- 6 volts
13	+ 6 volts
14	+ 6 volts
15	V1
16	V1
17	V1
18	V1
19	0v
20	0v
21	Sense V2
22	V2
23	V2
24	V2
25	V2
26	V2

Pin No.	Signal Name
27	0 volts
28	0 volts
29	0 volts
30	0 volts
31	0 volts
32	Sense 0 volts
33	Ref. Volts
34	0 volts
35	Volts correct
36	0 volts
37	Mains Earth

Socket 2 SKTD Store Unit to Margin Test Unit (DSMOO 12-14 SW)

Pin No.	Signal Name
1	0 volts
2	+ 5 volts
3	- 6 volts
4	+ 6 volts
5	V1
6	V2
7	+ 12 volts
8	V3
9	Spare
10	Spare
11	Inhibit Margins A
12	Inhibit Margins B
13	Inhibit Margins C
14	X Drive Margins A
15	X Drive Margins B
16	X Drive Margins C
17	Y Drive Margins A
18	Y Drive Margins B
19	Y Drive Margins C
20	Threshold Margins A
21	Threshold Margins B
22	Threshold Margins C
23	Spare
24	Spare
25	Indicator + 5 volts
26	In Limits
27	Spare
28	BL. 1

Pin No.	Signal Name	
29	BL.2	
30	BL.3	
31	BL.4	
32	BL.5	
33	BL.6	
34	BL.7:	
35	BL.8	
36	Spare	
37	Mains Earth	Screen

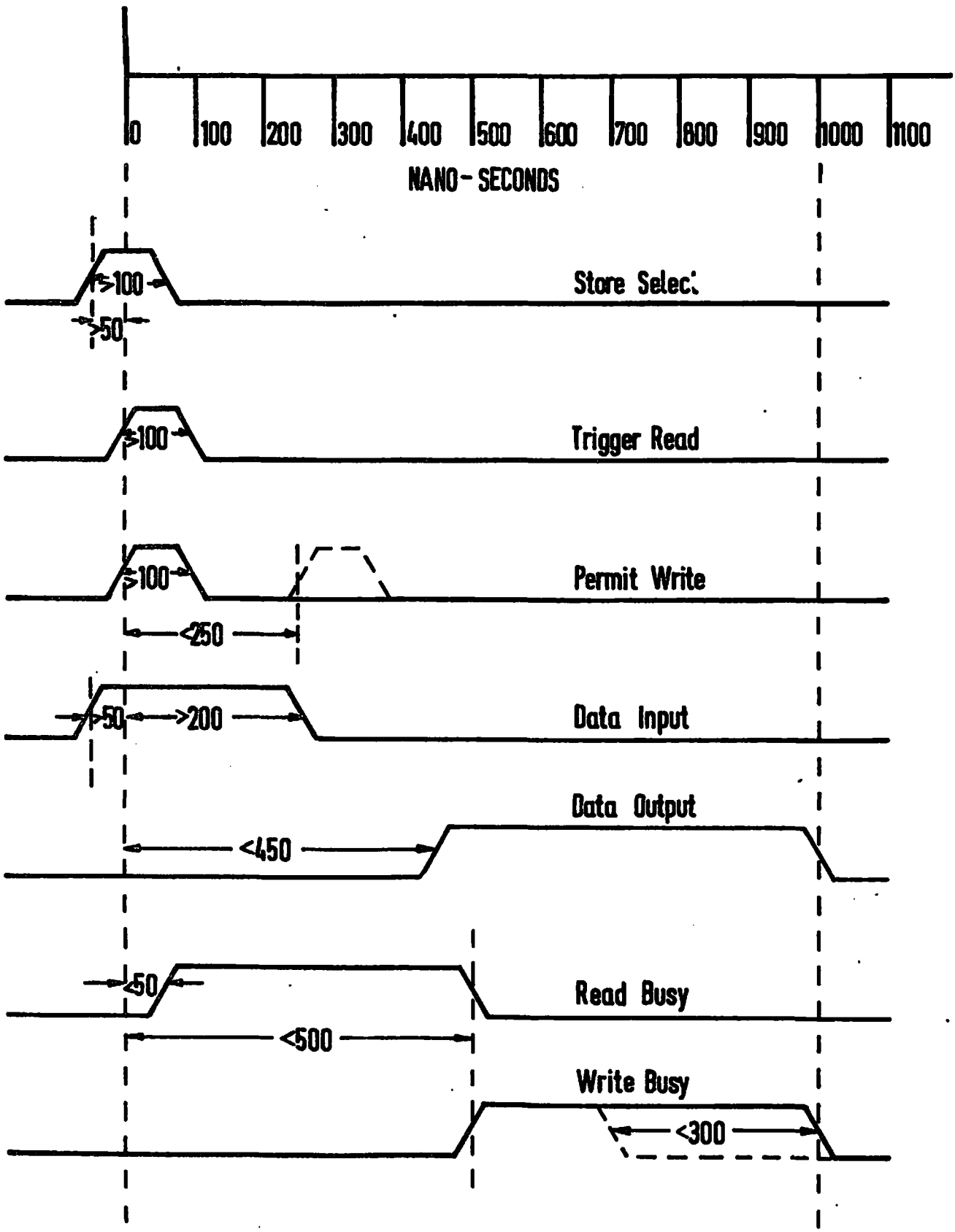


FIG. 2 READ / RESTORE CYCLE

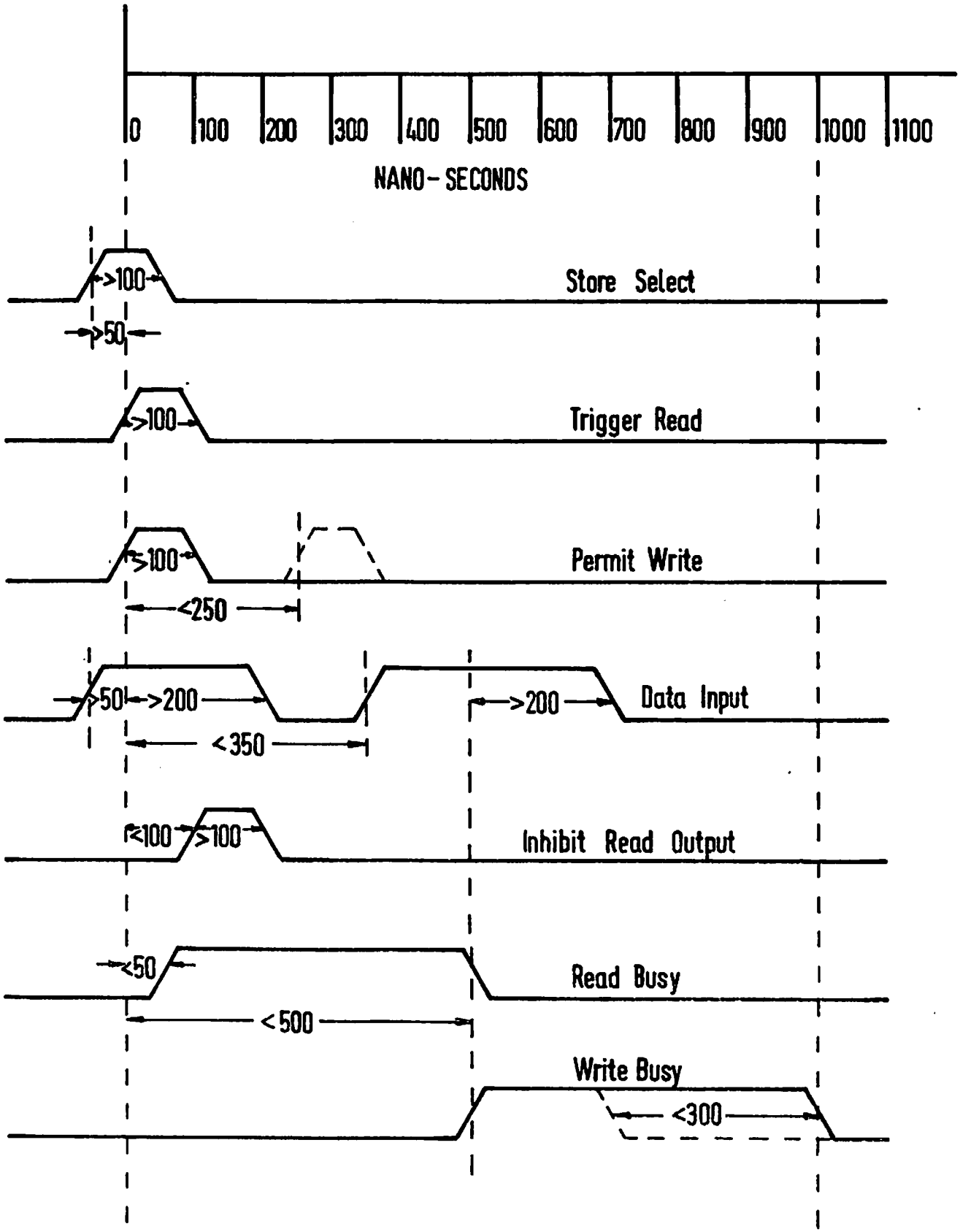


FIG. 3 CLEAR /WRITE CYCLE

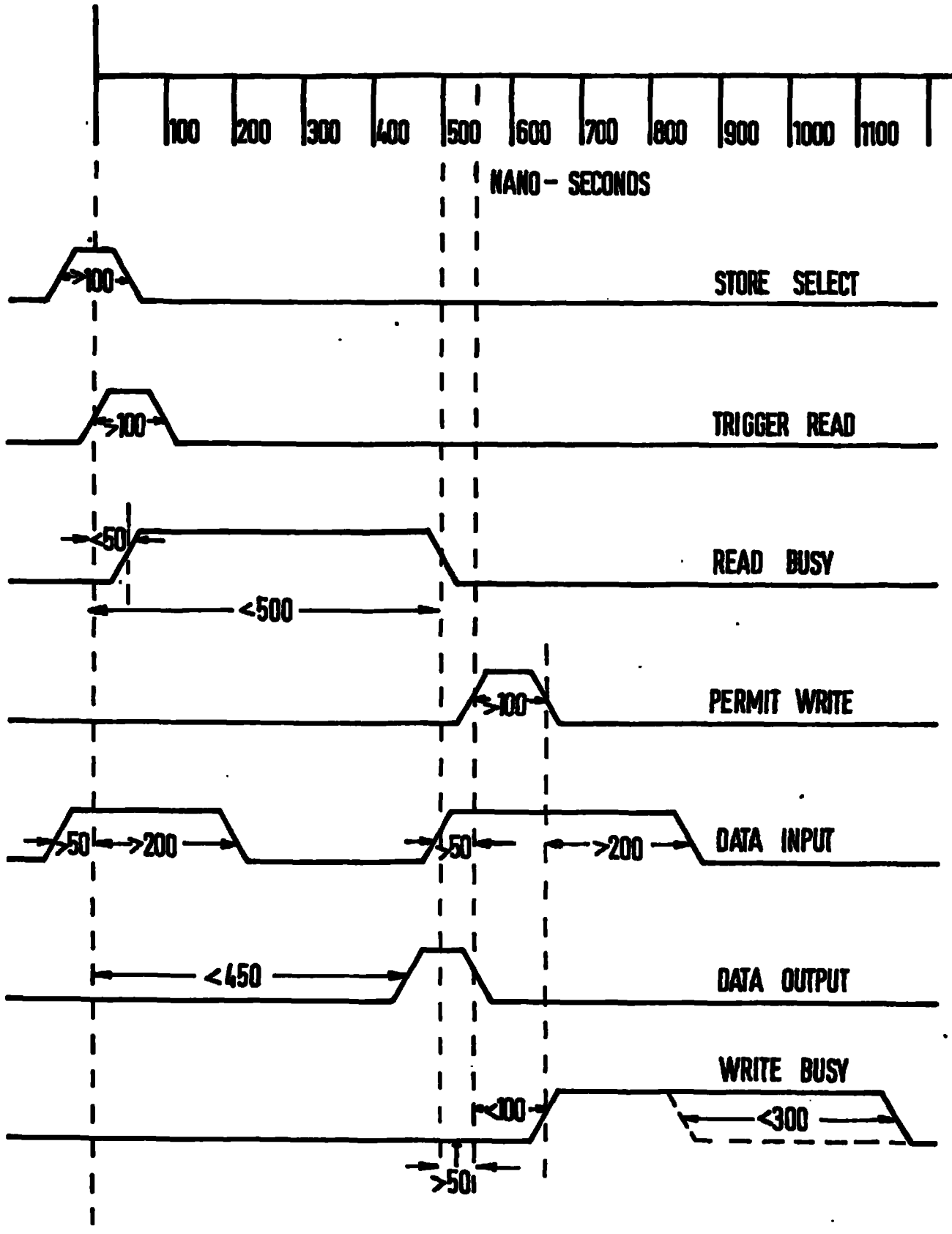
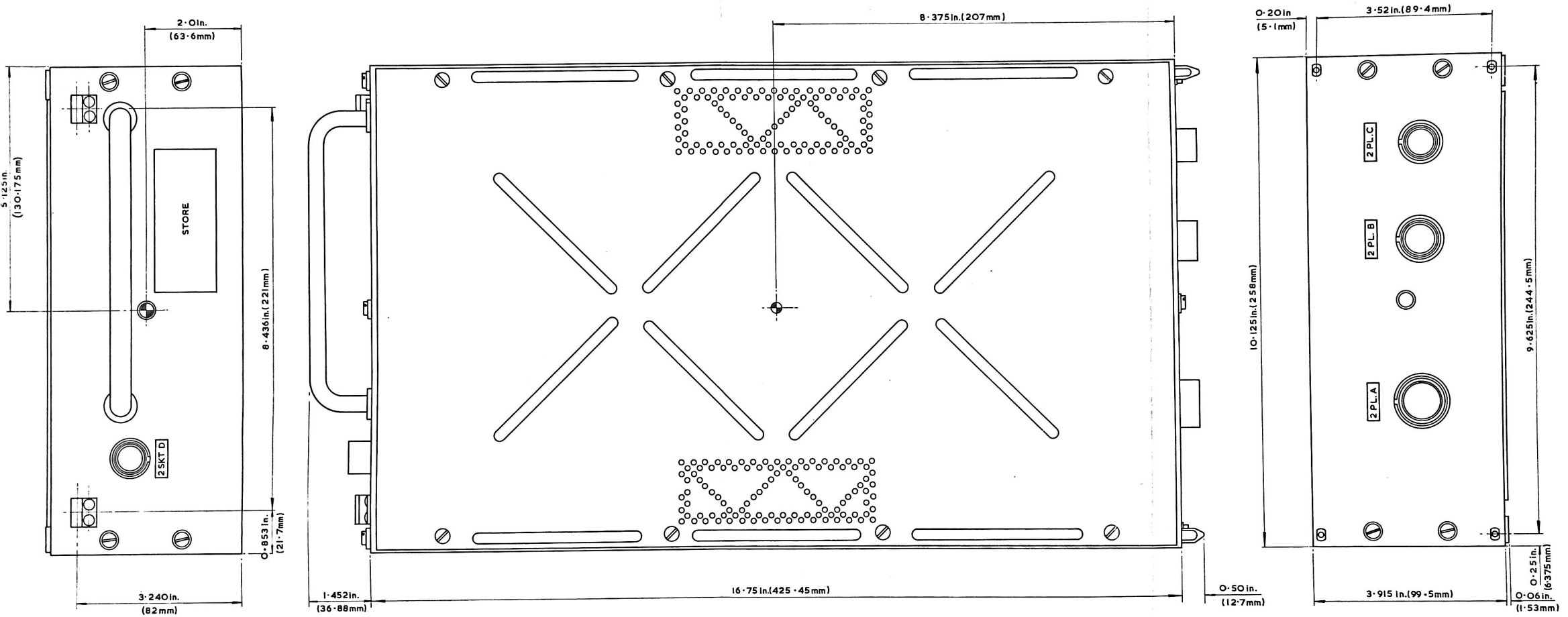


FIG. 4 READ-MODIFY-WRITE CYCLE



2 SKTD IS A HELLERMAN DEUTSCH CONNECTOR
37 WAY DS MOO 12-4-SW

NOTES:
1 ESTIMATED WEIGHT = 30lb (13·63Kg.)
2 CENTRE OF GRAVITY ESTIMATED & MARKED THUS ⊕

2 PLA IS A HELLERMAN DEUTSCH CONNECTOR
91 WAY DS MOO 27-30-PL.
2 PLB IS A HELLERMAN DEUTSCH CONNECTOR
61 WAY DS MOO 19-33-PW.
2 PLC IS A HELLERMAN DEUTSCH CONNECTOR
37 WAY DS MOO 12-14-PX.

INSTALLATION DRAWING – 8192 WORD 18 BIT 1 μs STORE
MCS 920C COMPUTER

322/SC16/8.68/1

SPECIFICATION

MCS 920C Memory Unit, 8192 words, 1 usec
Catalogue No. MCC 16.

1. Functional Specification

MCC16 is a store unit similar to the MCC 14 but supplied with terminating resistors fitted to the store highway lines. This provision enables a single store unit to be connected directly to a central processor without a 'T' -unit.

SPECIFICATION

MCS 920C Computer Power Supply

Catalogue No. MCC 21

1. FUNCTIONAL SPECIFICATION

1.1 Input

28V (nominal) DC. The unit will operate within specification over the input range 20 to 36 volts.

1.2. Output voltages.

1.2.1. The following stabilised DC outputs are provided:-

Supply	1.	+5 volts at 8·4A max. load	
"	2.	+5 volts at 9A " "	
"	3.	-6 volts at 1A " "	
"	4.	28 volts at 2·5A " "	
"	5.	+6 volts at 2·5A " "	The negative rail of this supply is connected to the positive rail of Supply 4 at the store.
"	6.	30 volts at 3A max. load.	This supply varies between 27 and 33 volts in direct linear proportion to a reference voltage, which is 8·5V when the output is 30V.

All supplies except Supply 5 have separate 0V lines.

1.2.2. Earthing

All output rails and control lines are isolated from the input rails and the chassis, but the independent 0V rails will be joined at the unit being supplied. The 0V sides of the output power rails are linked via 47Ω resistors with the logic ground rail in the power unit, (SKTF, pin 6).

1.2.3. Margin Testing

Supplies 1, 2, 3, 4 & 5 above are capable of variation by a preset control potentiometer, or margin test unit, over the range ± 10% of nominal. This facility applies only when the input voltage is within ±10% of 28 volts.

Supply 6: variation range 27 to 33 volts with 8·5V reference.

1.3. Controls

The unit has a remote ON/OFF switching facility controlled by two rails which, if connected together will switch the unit off, and if unconnected will switch the unit on, provided the input voltage is within the specified limits.

1.3.1. Switch ON Sequence

The outputs are sequenced on in the following order: Supplies 1, 2, 3, 4 come on within 100μsec of the ON signal. Supplies 5 & 6 come on after Supplies 1 to 4 have been established for 10 msec.

1.3.2. Power Supply Correct Signal

The unit provides a PSC signal which goes from 0V to +3V when all the outputs are within ±5% of nominal value. When in the positive state it is capable of supplying 75mA to the processor and/or stores.

1.3.3. Switch OFF Sequence

The switch-off sequence is in the reverse order to 1.3.1. Supplies 1 to 4 will switch off 50μsec after Supplies 5 and 6.

When the input voltage goes outside specified limits the unit will switch off as above.

1.4. Protection

(i) A 30A fuse, mounted on the front panel, protects the input supply.
(ii) All output supplies are protected against reverse polarity, short circuits, under and over-voltage.
(iii) No damage is caused if the input supply is connected in the wrong sense, or rises to 42 volts.
(iv) All supplies have current limiting set to 120% of their full load current.

1.5. Transients

The unit is capable of withstanding a steady input voltage of 42 volts, and transient voltages up to 82 volts. The unit has insufficient storage to run for 200msec while the input voltage is below 20 volts and therefore will not comply with BS2G 100. With the input voltage at 20 volts it will continue to operate within specification during a 200μsec interruption of the input supply.

1.6. Interference

Both input lines are adequately filtered to minimise RF interference and the unit is totally enclosed to reduce RF radiation. The radio interference generated by the unit is in general limited to the level required by AVP. 24 and BS. 2G. 100.

1.7. Reliability

The MTBF of the unit is better than 10,000 hours (calculated).

2. INTERCONNECTIONS

The unit is supplied with 4 plugs and sockets mounted on the rear panel, each marked with an identification label.

Pin numbers and connections are as follows:-

2.1. PLA (Hellerman Deutsch DSMOO 12 - 14 PY). Input Connector.

Pin	Function
1 - 15	Input positive
16 - 20	Spare
21 - 34	Input negative
35	Spare
36	Input negative
37	Mains earth

2.2. SKTB (Hellerman Deutsch DSMOO 12 - 14 SW). Output Connector.

Pin	Function
1 - 13	+5V 8·4A
14	Power ON +
15	Power ON -
16 - 27	0V (+5V 8·4A)
28	0V (-6V 1A)
29	-6V 1A
30 - 31	Spare
32	PSC +
33	PSC -
34	Timing margins 1
35	Timing margins 2
36	Timing margins 3
37	Mains earth

2.3. SKTC (Hellerman Deutsch DSMOO - 12 - 14 SX). Output to Store.

Pin	Function
1 - 5	+5V 9A
6 - 10	0V (+5V 9A)
11	0V (-6V 1A)
12	-6V 1A
13, 14	6V 3A
15, 16	0V (6V 3A)
17, 18	30V 2A
19, 20	0V (30V 2A)
21 - 26	30V 3A
27 - 31	0V (30V 3A)
32	Relay C
33	Reference voltage +
34	Reference voltage -
35	PSC +
36	PSC -
37	Mains earth

2.4. SKTD (Hellerman Deutsch DSMOO - 12 - 14 SY). Output to Store.

Pin	Function
1 - 5	+5V 9A
6 - 10	0V (+5V 9A)
11	0V (-6V 1A)
12	-6V 1A
13, 14	6V 3A
15, 16	0V (6V 3A)
17, 18	35V 2A
19, 20	0V (35V 2A)
21 - 26	30V 3A
27 - 31	0V (30V 3A)
32	Relay D
33	Reference voltage +
34	Reference voltage -
35	PSC +
36	PSC -
37	Mains earth

2.5. SKTE (Hellerman Deutsch DSMOO - 12 - 14 SY).
Margin test connector.

Pin	Function
1 - 3	Spares
4	0V (5V 8·4A)
5	+5V 8·4A
6 - 8	Margin (5V 9A)
9 - 11	Margin (-6V 1A)
12 - 14	Margin (6V 3A)
15 - 17	Margin (30V 2A)
18 - 20	Margin (5V 8·4A)
21 - 23	Spare
24	0V (-6V 1A)
25	-6V 1A
26	6V 3A
27	0V (6V 3A)
28	30V 2A
29	0V (30V 2A)
30	+30V 3A
31	0V (30V 3A)
32	+30V 3A
33	0V (30V 3A)
34	Protection override +
35	Protection override -
36	Spare
37	Mains earth

2.6. SKTF (Hellerman Deutsch DSMOO - 3 - 9 SX)

Pin	Function
1	Power On +
2	Power On -
3	PSC +
4	PSC -
5	Spare
6	0V (logic ground)
7	Mains earth

3. MECHANICAL CONSTRUCTION

The unit is a $\frac{1}{2}$ long ATR package, $16\frac{3}{4}$in. long. Weight is approx. 25 lb. The unit conforms to ARINC No. 404 and is paint finished matt black to DEF. 1059.

3.1. Cooling.

The unit is cooled by a fan mounted below the base which sucks air in from the top and out through the base.

4. ENVIRONMENT

The unit will operate within specification over an ambient temperature range of -10°C to +60°C, when supplied with an air flow of 60 lb/hr at the ambient temperature. Non-derangement storage temperature range is -40°C to +100°C.

4.1. Humidity

The operating humidity range is 0-95% RH.

4.2. Vibration

The unit will continue to operate within specification under vibration between 1 and 2000 C/S up to 10g., amplitude limited to 0·1 inch.

4.3. Shock

With an acceleration of 25g applied the unit will not break away from its mountings, nor become damaged internally.

4.4. Pressure

The unit will operate within specification at altitudes up to 60,000 ft, and will withstand the following pressure changes:

a) decrease of 25 p.s.i. per minute

b) increase of 20 p.s.i. per minute

SPECIFICATION

MCS 920 C Computer Power Supply 240V 50-60 c.p.s.

19" Rack Mounting, Standard

Catalogue No. MCC 24

1. FUNCTIONAL SPECIFICATION

1.1. Input

The unit provides stabilised output voltages to the computer from an A.C. mains input.

The input is provided with plug and socket tappings to enable units to work over the ranges:

200, 210, 220, 230, 240, 250 volts
100, 105, 110, 115, 120, 125 volts.

The unit operates over an input frequency of 50 or 60 c/s ± 10%.

1.2. Output Voltages

1.2.1. The following stabilised D.C. outputs are provided:-

Supply 1. +5V at 10A rating
" 2. +5V at 8A "
" 3. -6V at 1A "
" 4. +25-30V at 2·5A rating, adjustable in 1V steps
" 5. +6V at 2·5A rating. The negative output of this supply is connected to the positive of Supply (4).
" 6. 30V at 3A rating, capable of variation between 27V and 33V in direct linear proportion (within ±2%) to a reference voltage supplied to the power unit. This reference is 8·5V when the supply is at 30V nominal.
" 7. 30V at 3A rating, independent of Supply 6 and with a separate reference voltage.

Note: Only one of Supplies 6 and 7 will be loaded at any one time. The current ratings are as follows:

2.7A at 27V
3.0A at 30V
3.3A at 33V

All supplies except Supply 5 have separate OV lines.

1. 2. 2. Earthing

All output rails and control lines are isolated from chassis, but the independent OV supplies will be joined in the unit being supplied. In the MCC 24 unit, the OV side of the +5V 7A (Supply 1) is connected to mains earth (chassis) through a 47Ω resistor.

1. 2. 3. Margin Testing

Each of the outputs listed in 1. 2. 1 is capable of variation by a preset control potentiometer over the range -10% +15% of nominal. This facility is for use only when the mains input voltage is within ±3% of nominal.

1. 3. Controls

The unit is provided with a remote ON/OFF facility by means of relays, and supplies a control signal which prevents the contents of the store being corrupted on Switch ON or OFF.

1. 3. 1. ON-OFF Controls

The unit may be switched ON or OFF from the Control Unit by means of two control lines which, when connected together, switch the unit OFF, and when unconnected, switch the unit ON.

Switch ON occurs when contact is broken between Pins P and R of 5SKT B on the Power Unit.
Switch OFF occurs when contact is made between these pins.

The same function is also carried out by pins A & B of 5SKTF.

1. 3. 2. Power ON indication

An indicator lamp mounted on the front panel is illuminated when all supplies are within ±5% of their nominal values.

1. 3. 3. ON Sequencing

The outputs are sequenced on, in the following order:
Supplies 1, 2, 3, 4 come on instantaneously in response to the ON signal.
Supplies 5, 6, 7 come on after Supplies 1-4 have been established for 100 μS.

1.3.4. Power Supply Correct Signal

The unit provides a PSC signal which goes to +3V when all the outputs are within ± 5% of the nominal value. If conditions are not satisfied, the signal will be at 0 to 0.3V. When in the +ve state it is capable of supplying 75mA to the processor and/or store(s).

1.3.5. OFF Sequencing

The outputs are sequenced off in the reverse order to 1.3.3., i.e.:

Supplies 1-4 are not switched off until supplies 5-7 have been at less than 10% of nominal value for 100 µS.

1.3.6. Protection

(i) A mains fuse is provided in the primary of the mains transformer. A neon labelled "Mains Input", connected across the primary, is mounted on the front panel.

(ii) Each D.C. output is protected against internal short-circuit by a thermo-magnetic trip.

(iii) Each output has over and under-voltage and over-current protection. Over and under-voltage operate at ±10%, over-current at +50%, on nominal values.

(iv) A diode is fitted across each output to protect against accidental bias reversal by another power supply.

2. INTERCONNECTIONS

The unit is supplied with two cables as follows:-

(i) A 5-way mains input cable.

(ii) A 39-way cable max. 10ft long carrying D.C. supplies and control signals to the computer.

2.1. Connector Pin Schedules

2.1.1. Mains input connection, 5PLA, (Thorn PTO2A 14-5P)

Pin A	Line
Pin B	Neutral
Pin C	Mains Earth

2.1.2. Output Connections

Supplies 2,3,4 & 5 are common to two sockets, 5SKTC and 5SKTD. Supply 6 is routed through 5SKTC and Supply 7 through 5 SKTD.

5 SKTC 5 SKTD (Thorn PTO2A 20-39 SX) to Store Unit(s).

Pin	Signal
A-E	+5V at 8A (Supply 2)
F-K	OV at 8A " 2
L	OV at 4A " 3
M	-6V at 4A " 3
N,P	(+6V at 3A) " 5
R,S	(-6V at 3A) " 5
T,U	30-35V at 2A " 4
V,W	OV at 2A " 4
X	Sense 30V)
Y-c	+30V at 3A) " 6 or 7
d-h	OV at 3A)
i	Sense OV (Supply 6 or 7)
j	Ref. Voltage +ve
k	" " -ve
m	Supplies Correct +ve
n	" " -ve
p	Mains Earth

5 SKTB (Thorn PTO2A 20-39-SW) to Central Processor or I.C.U.

Pin	Signal
A-N	+5V at 7A (Supply 1)
S-d	OV at 7A " 1
e	OV at 100 mA
f	-6V at 100 mA[x]
g,h	Spare
i	Supplies correct (+ve)
j	" " (-ve)
k) Timing	Link to 5 SKTE Pin A
m) margins	" " " " B
n	" " " " C
p	Mains Earth
P	Power On (+ve)
R	Power On (OV)

[x] This supply is via a link from 5 SKTC or 5 SKTD. It is at -6V with respect to the OV side of Supply 1.

5 SKTE (Thorn PTO2A 20-39-SY) to Marginal Test Unit

Pin	Supply
A)	Link to 5 SKTB Pin k
B) Timing	" " " " m
C) margins	" " " " n
D OV	" " " " S (or equiv)
E +5V	" " " " A "
Y +5V (Sense)	" " " " g "
Z OV "	" " " " h "
a OV	" 5 SKTC " L "
b -6V	" " " " M "
c +6V (+41V)	" " " " N "
d OV (+35V)	" " " " R "
e +35V	" " " " T "
f OV	" " " " V "
g +27-33V	" " " " Y "
h OV	" " " " d "
i +27-33V	" 5 SKTD " Y "
j OV	" " " " d "
k	Protection override (+ve)
m	" " (OV)
p	Mains Earth

5 SKTF (Thorn PTO2A 10-6 S) To Control Unit

Pin	Signal
A	Power On (+) Link to 5 SKTB Pin P (or equiv.)
B	Power On (OV) Link to 5 SKTB Pin R(or equiv.)
C	Supplies Correct (+) Link to 5 SKTB Pin i (or equv.)
D	Supplies Correct (OV). Link to 5 SKTB Pin j (or equiv.)
E	Spare
F	"

3. MECHANICAL CONSTRUCTION

The unit weighs approx. 90 lb. and has a standard 19" front panel $10\frac{1}{2}$" high. Depth of chassis overall, excluding connectors, is 16"; maximum chassis width is $17\frac{1}{4}$". The case and front panel are stove enamelled dark grey to BS 2660-9-101.

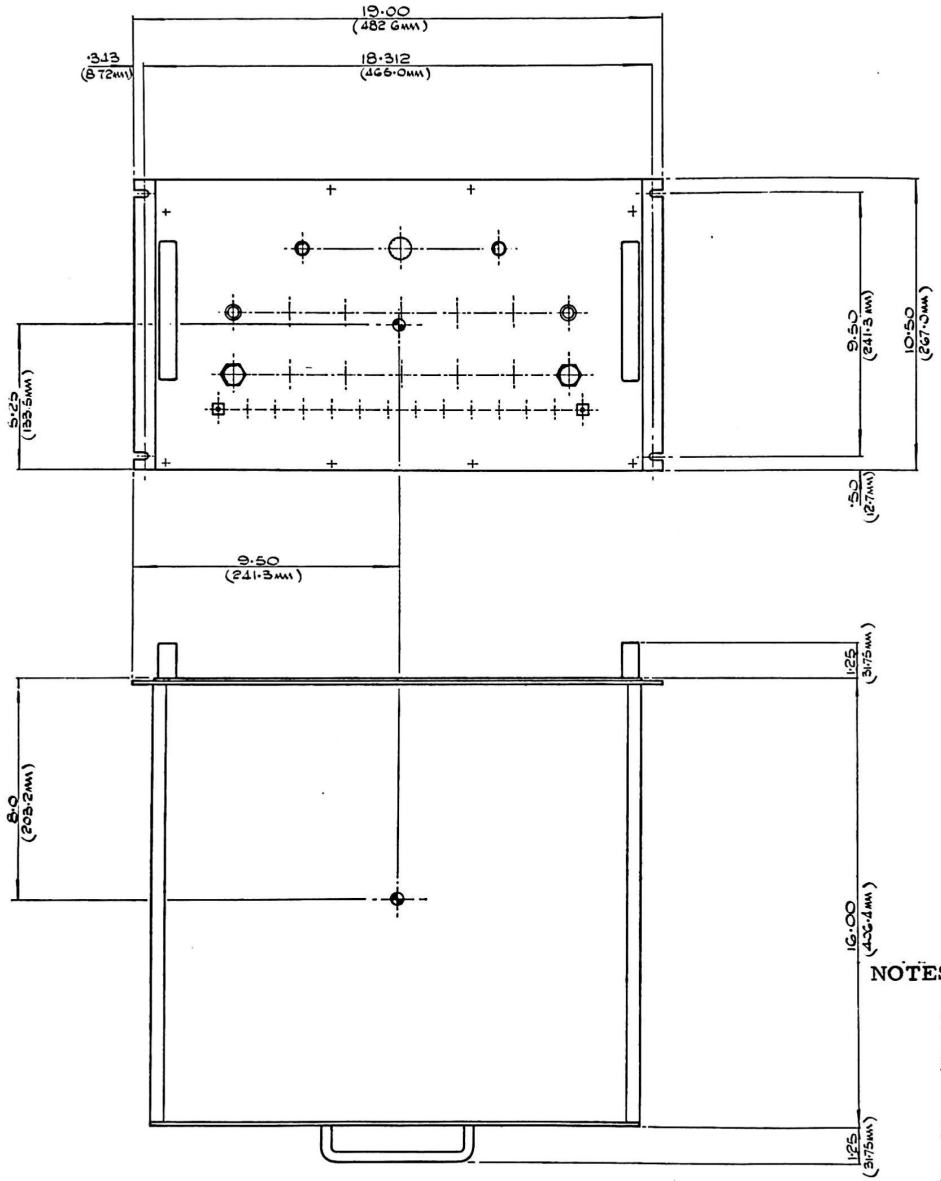
4. ENVIRONMENT

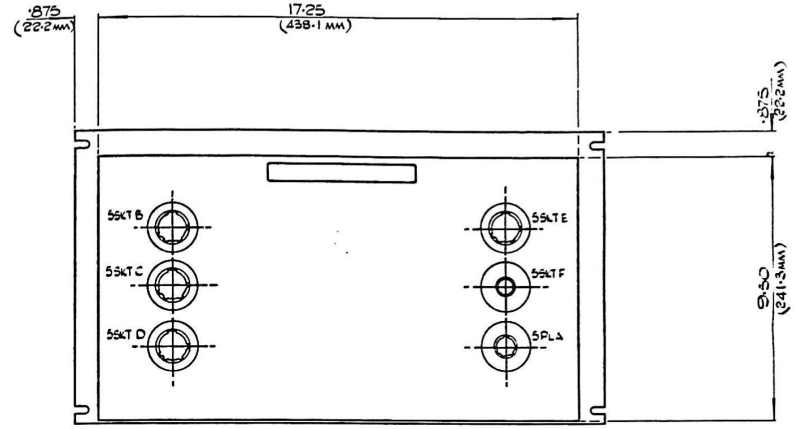
Construction is generally to DEF 133,LI. The unit will operate within specification over the temperature range 0 to +55°C

in still air, at a humidity of 0-95% RH. Non-derangement storage temperature is -40°C to +100°C.

4.1. Cooling

The unit is cooled by convection from its external surfaces, but the design provides for a supply of cooling air beneath the unit.





REAR VIEW

SSKT B	IS A THORN CONNECTOR TYPE PT02A-20-39SW.	SSKT E	IS A THORN CONNECTOR TYPE PT02A-20-39SX
SSKT C	IS A THORN CONNECTOR TYPE PT02A-20-39SX	SSKT F	IS A THORN CONNECTOR TYPE PT02A-10-6S
SSKT D	IS A THORN CONNECTOR TYPE PT02A-20-39SX	SPL A	IS A THORN CONNECTOR TYPE PT02A-14-5P

NOTES :-

1. METRIC EQUIVALENTS ARE APPROXIMATE
2. ALL DIMENSIONS ARE SUBJECT TO NORMAL MANUFACTURING TOLERANCES
3. CENTRE OF GRAVITY ESTIMATED & MARKED THUS:-
4. ESTIMATED WEIGHT = 85 lbs.

INSTALLATION DRAWING FOR:- COMPUTER POWER SUPPLY, MCC24. (322TD101)

SPECIFICATION

MCS 920C Computer

Primary Power Supply, 24V D.C. output

50-60 c/s Single-phase, Cat. No. MCC 28
400 c/s Three-phase, Cat. No. MCC 29

1. Functional Specification

The primary power supply unit, MCB 28, provides a 24V d.c. supply from a single-phase mains input of 100-125, 200-250 volts, 50-60 c/s, whereas MCB 29 provides 24V d.c. from an a.c. three-phase 400 c/s supply of 117 or 204 volts.

The unit incorporates a 4AH battery of nickel-cadmium cells, in the form of two encapsulated units, and a mains-operated charging unit.

1.2 Input

The input supply voltage and frequency range for MCB 28 are as follows:-

200, 210, 220, 230, 240, 250V ± 10%
100, 105, 110, 115, 120, 125V ± 10%
Frequency 45-65 c/s

The input supply voltage and frequency range for MCB 29 are as follows:-

117·5V ± 10% and 204V ± 10%
Frequency 360 -440 c/s

Neither unit will be damaged by a 50% increase in nominal supply voltage of 100mS duration.

1.2.1 Power Consumption

Under normal program running conditions the average input power is 600 watts. The maximum input power does not exceed 1 kilowatt. Up to 200 watts extra is consumed when charging the battery.

1.3 Output

1.3.1 The output voltage is 27V ± 0·5V under normal operating conditions with mains supply connected to the unit. Under mains failure conditions, the output voltage is 20-24V.

1.3.2 Full load output current is 24·5A.

1.3.3 The control voltage is 27·1V ± 0·3V at 20°C. Control voltage ripple is less than 120mV peak to peak with a load of 24·5A at 20°C. The control voltage varies linearly with battery temperature rise at a rate of -0·15% per degree C.

1.3.4 The unit is protected from damage by fuses if a short circuit is placed across its output.

1.3.5 The output voltage lines are isolated from chassis earth.

1.4 Power ON Indication

There are two indicator lamps mounted on the front panel:

(i) an indicator showing that the unit is connected to a live mains supply,

(ii) an indicator showing that the D.C. output is switched on.

Fuses mounted on the front panel are connected in the mains input circuit.

1.5 Operation

1.5.1 Input and output voltages are switched off simultaneously by an ON/OFF switch mounted on the front panel.

1.5.2 With the computer switched off by means of the Control Unit OFF button (MCC 40, 41) there is a drain of approximately 300mA on the Primary P.S.U. (MCC 28) to provide auxiliary supplies for ON/OFF sequencing and monitoring circuits in the computer power supply unit (MCC 21). To prevent battery discharge when the mains input power is removed, the ON/OFF switch described above (1.5.1) should be moved to the OFF position; the D.C. output will then be disconnected from MCC 21.

1.5.3 Nickel-cadmium batteries should not be stored for long periods at elevated temperatures in a charged condition since self-discharge of the cells may take place with consequent gassing of the battery when next charged.

1.5.4 At temperatures lower than -15°C gassing may occur if charging of a partially or fully discharged battery is attempted.

1.5.5 The battery should be stored in a discharged condition, i.e. at a fully discharged cell voltage of approximately 1·1 at 20°C. Do not discharge to zero volts as, owing to the differing cell capacities, some will have reverse polarity applied, which may cause gassing.

2. Interconnections

2.1 Input connector, Thorn PTO2A-14-SPW (8 PLA):

	MCC 28	MCC 29
Pin A	Line	Line (red)
" B	Neutral	Spare
" C	Mains Earth	Mains Earth (chassis)
" D	Spare	Line (yellow)
" E	"	Line (blue)

2.2 Output connectors (2) Thorn PTO2A-20-39SW (8SKT B, 8SKT C)

Pins A-R	Positive output
" Z-k	Negative "
" n-q	" "
" r	Mains Earth (chassis)
" S-Y, m	Spare

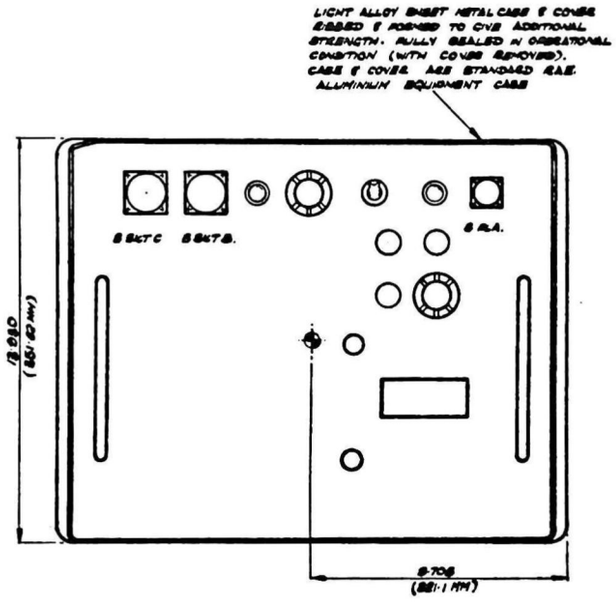
3. Mechanical Construction

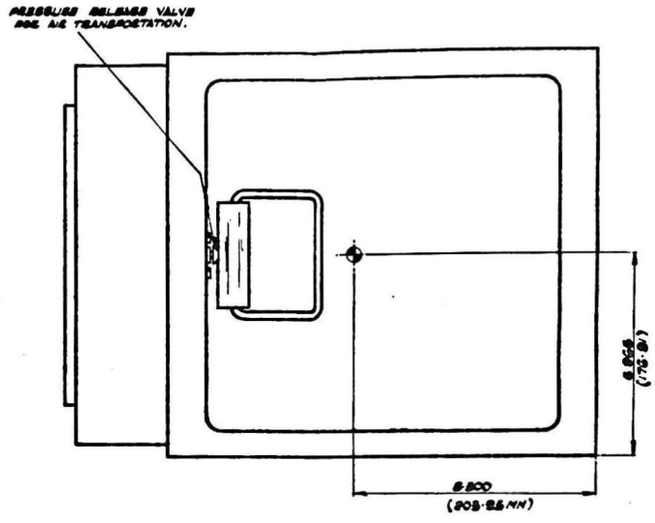
The unit is housed in a size 25s RAE aluminium instrument case, complete with chassis runners and spigots. The dimensions are as on MCD drawing No. 322 TD 103, weight approximately 110lbs. Two $\frac{3}{4}$" diam. holes are provided in the front panel to allow the batteries to vent to atmosphere.

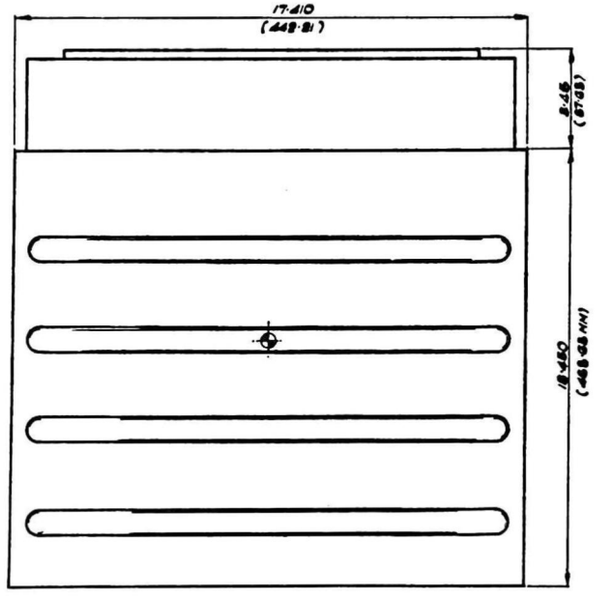
The paint finish for military use is semi-gloss to DEF 1059, front panel and all internal surfaces eggshell black, other external surfaces in colour BS 2660-9-094.

4. Temperature range and environment

The unit is designed for use in military and rugged commercial environments. It will meet specification over a temperature range of -20°C to +45°C ambient. It will also operate between -40°C and +55°C, meeting the specification in all respects except MTBF, which has been calculated to be not less than 8000 hours.







NOTES :-

1. METRIC EQUIVALENTS ARE APPROXIMATE
2. ALL DIMENSIONS ARE SUBJECT TO NORMAL MANUFACTURING TOLERANCES
3. CENTRE OF GRAVITY ESTIMATED & MARKED THUS :-
4. ESTIMATED WEIGHT = 110 lbs

8PLA IS CONNECTOR THORN TYPE PTOOE 14·5P OR EQUIVALENT MATING PART IS CONNECTOR THORN TYPE PTO5A-14-5S OR EQUIVALENT.

8 SKTB & 8 SKTC ARE OUTPUT CONNECTORS THORN TYPE PTO2A 20-39 SW OR EQUIVALENT. MATING PART IS CONNECTOR THORN TYPE PT06E 20-39 PW.

INSTALLATION DIAGRAM PRIMARY POWER SUPPLY SINGLE PHASE 50-60c/s MCC 28, 29. (322TD083)

322/SC38, 39/8. 68/1.

SPECIFICATION

MCS 920C Computer, Mains Filter Units
Catalogue Nos. MCC 38, 39.

These filter units are purchased from Belling Lee Filtron Ltd. and are identical to the corresponding MCB units. MCC 38 is for 400 c/s, MCC 39 for 50 c/s mains supplies.

SPECIFICATION

MCS 920C CONTROL AND MONITOR UNIT

Catalogue No. MCC 40,41.

1. General Description

The 920C Control and Monitor Unit (Catalogue Nos MCC 40 and MCC 41) forms part of the MCS 920C Computer System, and has similar control facilities to other 920 Series computers. In the 920C unit however, both the control and the monitoring facilities are housed within one unit.

The system units associated with the Control and Monitoring Unit, in a typical system, are as follows:-

Central Processor, Store Unit, Interface Control Unit, Teleprinter and Paper Tape Units, Power Supply Unit.

The Control Unit is basically an item of test equipment, to permit control of the central processor independently of its peripheral system. In certain applications it may be used as an operational control panel. The unit features a single mode switch, which controls the power supply throughout a system, and ergonomic grouping of the controls and indicators. The eighteen indicators, in conjunction with a selector switch, are capable of monitoring 196 different waveforms.

The Control and Monitor Unit is manufactured both as 19" rack mounting equipment (MCC 40) and as a free standing unit (MCC 41). Both types will satisfy the requirements of Specification DEF 133, Class L1.

2. Functional Specification

Connection of the Control and Monitor Unit to the central processor transfers from the power supply unit its automatic control of power ON/OFF, and places it under the direct control of the operator. Control is effected by operating the 'ON' switch mounted on the control face of the unit. The control facilities and monitor indications which are then available to the operator are detailed below.

Disconnection of the control unit from the processor will allow the automatic control of switch ON/OFF within the power supply unit to function. On switch ON, the processor will automatically start obeying program in store location 8177. If however the paper station is connected, then initial instructions will be obeyed at address 8181.

2.1 Master Mode Switch

The control facilities of the unit fall into three groups as governed by the three positions of the master switch. The modes are: AUTO, MANUAL, AND TEST. The switch is key operated, the key being trapped in the TEST mode.

Where this switch renders particular controls ineffective, the computer operates as if those controls were in their 'normal' state. The control unit is designed so that the 'normal' state for:-

INTERRUPT:	will only allow external interrupts to be enabled;
LOCK-OUT:	protection will be in operation;
ERROR-STOP:	will be disabled, the computer will continue to run if store lock-out or parity errors are generated.

2.1.1 Auto

In this mode only the ON/OFF and Volume controls are operative, although all lamp indications and loudspeaker monitor circuits still function.

In this mode, operation of the ON button causes the computer to start automatically obeying program at location 8177.

2.1.2 Manual

The computer enters the 'Reset' state on switching ON; operation of the Jump key causes the computer to start obeying program at the location set up by the number generator.

In this mode routine operation of developed programs is enabled. The following controls will be available:

Number generator keys
Jump, Restart, Stop, Reset,
Program level controls

The functions of these switches are detailed later.

These controls enable the reading of new programs and the checking of programs by use of the TRACE facility.

2.1.3 Test

The Computer operation on Switch ON is the same as Manual.

In this mode, the remaining controls on the panel become operative, in addition to those of 2.1.3 and 2.1.2. They are ENTER, OBEY, CYCLE ORDER STOP, CYCLE REPEAT.

These provide the extra facilities required by an engineer for fault tracing, program check-out, and maintenance.

2.2 Power ON/OFF Switch

Power control throughout a 920C system is effected by a single shrouded switch. This is operative in all modes of the Auto-Manual-Test switch.

2.2.1 OFF

This operation of the switch initiates a controlled shut-down which switches off the power in correct sequence and timing, to ensure the contents of the store are not lost.

2.2.2 ON

This operation of the switch initiates a controlled system switch-on sequence. When the processor power supply is switched on and within operating limits, the 'Power On' Lamp is illuminated (Green). When all interlocked units in the system are switched on and at their correct operating level, the 'Ready' lamp is illuminated (Green).

2.3 Number Generator

This consists of 18 key switches corresponding to the 18 bits of the computer word. Depression of a key corresponds to a one (1).

The number generator can be used for three purposes, viz:-

2.3.1 Address for JUMP operation will be initiated by raising the JUMP switch to the UP position. In this case only bits 1-13 are effective, and they specify the location to which the jump is to be made, causing the computer to start obeying a program on level 1.

2.3.2 Number to be entered into the Accumulator or A register of the computer. All 18 bits specified by the keys will be copied into the Accumulator when the ENTER control is operated.

2.3.3 Instruction to be obeyed when the OBEY control is operated. All 18 keys will be operative - thus a modified instruction (bit 18) may be set up and obeyed directly.

2.4 Manual Controls

This group consists of six controls (Stop, Restart, Reset, Jump, Lockout, Error Stop) which initiate operations in the computer.

2.4.1 Stop

This is an illuminated push button. Its operation will stop the computer at the end of its current instruction. The control is ineffective in the Auto mode. The push button is illuminated (red) when the computer has stopped. The stop condition may be terminated by operation of the RESTART or JUMP controls.

2.4.2 Restart

This is a push button switch. Its operation will restart the computer after being stopped by the action of 2.4.1. It is inoperative in the AUTO mode.

2.4.3 Reset

This is an illuminated push button switch. Its operation will cause the computer and peripherals to be reset and remain in this state until the 'JUMP' control is operated. In the active state the push is illuminated (amber).

2.4.4 Jump

This is a three position switch which when raised will initiate a jump instruction to the address set up on the number generator keys, bits 1-13. (see 2.3.1.) If the computer is running, it will still effect a jump to the new level.

Depression of the switch will initiate a jump instruction causing the computer to start obeying the initial instruction on level 1.

2.4.5 Lockout

2.4.5.1 Lockout Switch and Lamp

This is an alternative action push button switch. When the push button is depressed and the 'Lockout' lamp (upper half, green) is illuminated store protection is brought into operation. When the lamp is not illuminated store protection is disabled.

2.4.5.2 Lockout Error Lamp

This is illuminated (lower half, red) when the processor stops because of an attempt to over-write a protected word.

2.4.6 Error Stop

2.4.6.1 Error Stop Switch and Lamp

This is an alternate action push button switch. When the push button is depressed and the lamp (upper half, yellow) is illuminated the processor will stop if a store parity error is detected or when store protection is in operation and an attempt is made to over-write a protected word. When the lamp is not illuminated the processor will not stop on errors.

2.4.6.2 Parity Lamp

This is illuminated (lower half, red) when the processor stops on a store parity error.

2.5 Program Level Controls

These controls comprise three illuminated push button micro-switches and three associated level key switches. One push button switch and one key are associated with each of the three program levels, 1, 2, & 3.

2.5.1 When a key switch is down, the associated level is set to Manual and external interrupt signals will not be recognised. When set to the up position, a permanent interrupt condition is generated for use with the TRACE program.

2.5.2 In the intermediate position, the switches allow on-line operation of the computer, i.e. it will recognise external interrupt signals.

The push buttons are effective only when the corresponding level is set to 'manual'. In this case operation of the button generates one interrupt condition. On receipt of this interrupt demand by the computer, the upper half (red section) of the push button is illuminated. The lower half (green) will light when the corresponding program level is being obeyed i.e. Active.

2.6 Test Controls

This group of controls is operative only in the TEST mode. They permit the engineer to enter new programs, obey, and if necessary test operations, step by step throughout the course of a program. Each control is a three position switch (centre normal) except the Cycle Repeat switch.

2.6.1 Enter

Setting this control will permit copying the number set up on the number generator keyboard, as shown by the indicator lamps, into the A register of the computer upon operation of the 'RESTART' button. The 'Enter' switch may be raised to the 'run' position (after the first restart, the number generator will be copied continuously) or may be lowered to the 'single' position, in which case the number on the keyboard will be entered once, and the computer will then stop.

2.6.2 Obey

Operation of this switch will cause the computer to obey the instruction set up on the number generator keys, as shown by the indicator lamps.

The control is a three position switch. In the raised position the instruction is obeyed continuously and in the lowered position the instruction is obeyed once, after operation of the Restart button.

Operation of the 'Obey' switch in the SINGLE position will simultaneously give 'Obey' and 'Order Stop' instructions.

2.6.3 Order Stop/Cycle Stop Keyswitch

In the lowered position of this control the computer will be set to the 'Order Stop' state, in which it will obey a stored program one instruction at a time. Each successive order is initiated by operation of the 'RESTART' button.

In the raised position, the computer will be set in the 'Cycle Stop' state, in which the computer obeys successive steps in the microprogram each time 'RESTART' is operated. The 'STOP' lamp will be illuminated when the control switch is raised or lowered, remaining alight until normal operation is resumed, on selecting the centre switch position.

2.6.4 Cycle Repeat

When this key is set to the raised position, the computer will obey a single instruction in the micro-program repeatedly.

If Cycle Stop is set, repetition will occur each time the RESTART control is operated. If Cycle Stop is not set, repetition occurs continuously.

2.7 Monitor Display Switch and Indicator Lamp

The eighteen indicator lamps, in conjunction with the eleven position selector switch, enable the state of all central processor registers, important staticisors, and control logic waveforms to be displayed to the operator. This facility is basically part of computer test equipment, but may be used when setting up a new system.

The waveforms available to the operator are grouped below; those waveforms required for testing or fault finding (7 to 11) are detailed in the appendix.

Display Switch Position	Waveform Groups Displayed
1	Register Bits P1-P13; I14-17; Qo
2	Register Bits Q1-18
3	Register Bits A1-18
4	Register Bits S1-17; H staticisor
5	Register Bits J1-17; T staticisor
6	Register Bits M1-18
7	16 Control matrix steps and Timer Waveforms
8	)
9	) 4 times 18, control output waveforms for
10	) computation and store access.
11	)

2.8 Audio Monitor Equipment

An amplifier, volume control and loudspeaker are provided in the unit. The loudspeaker emits an audible indication that the computer is running, the pitch of the note is controlled by the rate at which jump instructions are obeyed by the central processor.

Appendix A

Central Processor Microprogram Control Waveforms available for Display

Display Switch Positions	Abbreviated Waveform Identification	Control Waveform Detail and/or Function
7	S0 to S8	Microprogram sequencing steps
	I0 to I2	Interrupt " "
	NG0	Word generator " "
	BT	Block Transfer Staticisor
	LW	Last Word "
	TA:TB	Timer Flip Flop output A;B
	MKR	Block Marker Staticisor
8	ADT 1 to 5	Autonomous Access Request Staticisors
	PTA1; PTA2	Input peripheral to A reg; Input paper tape
	RTA; FTA	Shift A reg. 1 place right; Input adder to A reg.
	WTX; QTX	Input word generator to X bus; Output Q reg to X bus
	VTA; 1TF	Input collated bits to A reg; Increment Adder.
	TRB; TRI	Store busy staticisor; clear store cycle staticisor.
	PR; RPT	Permit read staticisor; cycle repeat
	2MTY	Output twice contents of M reg to Y bus.
9	Z1; Z2	Peripheral request staticisor; Peripheral reply.
	PROC; EXT	Processor store cycle; Extract: read next instruction.
	FTQM; QSR	Input adder bits 14-18 to Q reg; Shift Q 1 place right
	FTS; STY	Input Adder to S reg; Output S reg to Y bus.
	2RTA; A = 0	Shift A reg 2 places right; A reg contents zero.
	LTA; ETJ	Shift A reg 1 place left; Input address of S reg to J reg.
	FTM; FTI	Input Adder to M reg; Input Adder to 1 reg.
	ATX; $\bar{A}$TX	Output A reg to X bus; Output inverse A reg to X bus.
	FTT	Retention of A Bit 19 during division
	TR, M	Select M reg and generate trigger Read pulse
10	F19; F20	Overflow Bits retained in Adder
	QS2R; QSL	Shift Q 2 places right; Shift Q one place left

Display Switch Positions	Abbreviated Waveform Identification	Control Waveform Detail and/or Function
	SITS; SITJ	S increment to S reg; S increment to J reg.
	JITJ; SITMQ	J increment to J reg; S increment to M and Q reg.
	INT; K1	Interrupt current level; Increment Store Address reg.
	TR, IRO	Generate Trigger Read and Inhibit Read Out pulses
	JTYM; JTYL	Output J bits 14-17 to Y bus; Output J bits 1-13 to Y bus
	MTYM, MTYL	Output M bits 14-18 to Y bus; Output M bits 1-13 to Y bus
	RCP; FTQL	Reset current program; Input adder bits 1-13 to Q reg.
	$\overline{2M}$TY	Output twice contents of M reg inverted to Y bus
11	SEL A-S	Select A,Q,I,M,J or S reg.
	SEL E	Select E: Program level demand staticisors
	SEL H	Select H: Address mode staticisor
	SEL TB	Select TB: Select store unit
	EWC; II	End of write cycle; Initial Instructions
	FTJL; FTJM	Input Adder Bits 1-13 to J reg; Input Adder Bits 14-17 to J reg
	$\overline{MT}$Y	Output Inverse contents of M reg to Y bus
	MTP; NEXT	Output M reg to P reg; Next instruction.
	ST.TM; II TM	Stop timing pulse; Initial Instruction timing pulse.

3. Interface Specification

Introduction:

The 920C Control and Monitor Unit incorporates three connectors, two of which provide the interface to the Central Processor; and the third is used to interconnect the ON/OFF control lines of a second Power Supply Unit, when required in a system.

3.1 Central Processor Interface

3.1.1 Control Interface Signals

One connector is used for all control signals to and from the processor, and also for the small number of 'through' signals terminating in the store and power supply units. The function and direction of the control signals at the interface are given below.

3.1.1.1 Auto/Manual/Test

To processor, one line each. The appropriate signal will only be set to the true state when selected on the Mode switch. For normal operation the AUTO mode will be selected, and the MANUAL and TEST lines will be false.

3.1.1.2 Word Generator

To processor, eighteen lines. These lines carry the binary digits that form a number to be transferred, or an instruction to be obeyed by the processor. A line is set to its logic '1' only when the appropriate key is depressed (except when the JUMP control is operated). Each line will normally be set to the logic 'O' state.

3.1.1.3 Enter/Obey

To processor, one line each. Each line will only be set false when the appropriate control is operated, causing the processor to enter a word into its A register, or obey the instruction set on the word generator keys. The lines will normally be set true.

3.1.1.4 Cycle Repeat

To processor, one line. The line when set false will cause the processor to obey a single microprogram instruction repeatedly. The line will normally be set true.

3.1.1.5 Cycle Stop/Order Stop

To processor, one line each. A line when set false will cause the processor to obey the appropriate single microprogram or stored program instruction and stop. Each line will normally be set true.

3.1.1.6 Jump S.S.

To processor, one line. This line when set to the true state will cause the processor to start obeying program instructions. The line will remain true for a nominal 30 microseconds, and will then become false. The line will normally be set false.

3.1.1.7 Reset S.S.

To processor, one line. This line when set to the true state will cause the processor to enter the reset state. The line will remain true for 2 microseconds and will then become false. The line will normally be set false.

3.1.1.8 Restart S.S.

To processor, one line. This line when set to the true state will cause the processor to restart. The line will remain true for 2 microseconds and will then become false. The line will normally be set false.

3.1.1.9 Manual Interrupts

To processor, three lines. A line when set false will cause the processor, on the appropriate level, not to recognise an external interrupt signal. Each line will normally be set true.

3.1.1.10 Permanent Interrupts

To processor, three lines. A line when set false will cause the processor, on the appropriate level, to remain in a permanent interrupt state. Each line will normally be set true.

3.1.1.11 Level Interrupts S.S.

To processor, three lines. A line when set to the true state will cause the computer to recognise, on the appropriate level, the demand for change of program. The line will remain true for 2 microseconds and will then become false. Each line will normally be set false.

3.1.1.12 NG2 and NG2-1

To and from processor, one line each. The NG2 line when set true will set the normally '0' logic terminal of word generator bit 17 to a logic '1'. When NG2 is set false, the terminal is set to a logic '0' state. The NG2-1 line is connected to the NG2 line, and both lines will exhibit the same logic state. The lines will normally be set true.

3.1.1.13 Lockout

To processor, one line. The line when set false will cause store protection to be brought into operation. The line will normally be set false and may only be set true, when operating in 'Manual' or 'Test' modes.

3.1.1.14 Error Override

To processor, one line. The line when set true will cause the processor not to stop on store errors. The line will normally be set true and may only be set false when operating in 'Manual' or 'Test' modes. .

3.1.1.15 On Switch

To processor, one line. This line when set false will cause the power supply unit to shut down all power lines. The line will normally be set true.

3.1.1.16 Demand Levels

From processor, three lines. A line when set true will cause the appropriate level 'Demand' indicator to become illuminated. Each line will normally be set false and is only set otherwise when a change in program is required.

3.1.1.17 Active Levels

From processor, three lines. A line when set true will cause the appropriate level 'Active' indicator to become illuminated. A line is set true when appropriate level of program is being obeyed, at all other times the line will be false.

3.1.1.18 Control Indicators

From processor, four lines. The line when set true for:

Ready, On, Stop, Reset; will cause the appropriate indicator to become illuminated. The 'Ready' and 'On' lines will normally be set true; the 'Stop' and 'Reset' lines will only be set true when the processor is in, respectively, a stop or reset state.

3.1.1.19 Error Indicators

From processor, two lines. The line when set true for: Parity Error, Lockout Error, will cause the appropriate indicator to become illuminated. Both lines will normally be false, and are only set true whenever an error is detected in the store.

3.1.1.20 Audio

From processor, one line. The line is set true whenever the processor performs a jump function, and causes the loudspeaker to emit a higher note. The line will normally be set false.

3.1.2 Monitor Interface Signals

One connector is used for all the monitor signals to and from the processor. The function and direction of the signals at the interface are given below.

3.1.2.1 Monitor Indicator Signals

From the processor, eighteen lines. These lines are designated MON 1 to 18 and connect to lamp drivers within the C.M.U. A line when set true, causes the appropriate indicators to become illuminated. The state of each line is undefined.

3.1.2.2 Monitor Select Signals

To the processor, eleven lines. These lines are designated MON A to C3 and the state of a line is determined by the Display switch on the C.M.U. A line, when set true, selects the appropriate group of eighteen processor control waveforms, to be displayed. Lines will normally be set false.

3.1.3 Power Supply Interface Signals

A seven way connector is provided, for use when the system requires a second power supply unit, in order that both power units may be controlled from the same source. The function and direction of the signals are given below.

3.1.3.1 Power On

To (additional) power supply unit, one line. This line when set false will cause the power supply unit to shut down its power lines. The line will normally be set true.

3.2 Interface Connection Details

The interconnection details between the control unit and the processor and additional power supply unit are given below:-

3.2.1 Central Processor/Control and Monitor Unit Connection Schedule

Plug A

Control Unit fixed connector: Hellerman Deutsch, DSMOO 27-30 PW
Cable free connector: Hellerman Deutsch, DSMO7 27-30 SW 004

Control Unit Plug Pin	Function	Control Unit Plug Pin	Function
1	Active 1 = Lamp	41	PERM INT 3
2	" 2 = Lamp	42	LOCKOUT
3	" 3 = Lamp	43	CYCLE REPEAT
4	0 Volts	44	OBEY
* 5	S.S. Level 1	45	Word Gen: Bit 5
* 6	Level 2	46	" 12
* 7	Level 3	47	" 4
8	Manual or Test	48	" 3
9	Lockout Error	49	" 9
10	Parity Error	50	" 2
11	+5 Volts	51	" 1
12	ON Switch signal	52	" 11
13	Return for pin 12	53	" 10
14	+5 Volts	54	" 13
15	ORDER STOP	55	0 Volts
16	NG2	56	Word Gen: Bit 17
17	Word Gen: Bit 18	57-66	0 Volts
18	" " 16	67	AUDIO
19	" " 15	68	Stop: Lamp
21	" 6	69	Reset: Lamp
22	" 14	70	-6 Volts
23	" 7	71	Spare
24	" 8	72-76	+5 Volts
25	NG2 - 1	77-80	Spare
26	Ready	81	-6 Volts
27	AUTO	82	Spare
28	Power ON: Lamp	83	ERROR OVERRIDE
29	Demand 2: Lamp	84	Spare
30	" 1: Lamp	* 85	RESET SS
31	" 3: Lamp	86-87	Spare
32	ENTER	88	Spare
* 33	JUMP SS	89	Spare
34	PERM INT 2	°90	0 Volts
35	MAN INT 3	91	Mains Earth
36	MAN INT 2		
37	CYCLE STOP		
* 38	RESTART S.S.		
39	MAN INT 1		
40	PERM INT 1		

* Single coax cable required in cable form
° Connect to outer braid of cable form

3.2.2 Central Processor/Control and Monitor Unit Connection

Schedule: Plug B

Control Unit fixed connector: Hellerman Deutsch, DSMOO 12-14 PX
Cable free connector " " DSMO7 12-14 SWOO

Control Unit Plug Pin	Function	Control Unit Plug Pin	Function
1	Mon 1	19	0 Volt
2	" 2	20	Mon A
3	" 3	21	Q
4	" 4	22	P
5	" 5	23	M
6	" 6	24	J
7	" 7	25	S
8	" 8	26	T1
9	" 9	27	T2
10	" 10	28	C1
11	" 11	29	C2
12	" 12	30	C3
13	" 13	31) ...	0 Volt
14	" 14	32)	
15	" 15	33)	
16	" 16	34) ...	+5 Volts
17	" 17	35)	
18	" 18	* 36	0 Volt
		37	0 Volt

* Connect to outer braid of cable form

3.2.3 Power Supply Unit/Control and Monitor Connection

Schedule: Plug C

Control Unit fixed connector: Hellerman Deutsch, DSMOO 3-9 PX
Cable free connector: " " DSMO7 3-9 SX OO4

Control Unit Plug Pin	Function
1	Power On: Signal
2	Power On: Return
3	Spare
4	Spare
5	0 Volts
* 6	0 Volts
7	Spare

* Connect to outer braid of cable form

4. Power Supplies

Supplies for the Control and Monitor Unit are derived from the computer and comprise:-

+ 6V

Common 0V

- 6V

5. Mechanical Construction

The unit is available in two forms. In the rack-mounting version (MCC 40), the dimensions are as follows:

Width: 19" (482.6 mm.)
Height: 7" (177.8 mm.)
Depth: 8.66" (220. mm.)

(Overall, including connectors but not handles)

Weight: approx. 12 lb.

See installation drawing 322T059.

The free-standing version (MCC 41) is 19.6" wide x 7" high x 7.2" deep (approx.)

Weight: approx. 15 lb.

6. Environmental Specification

6.1 General

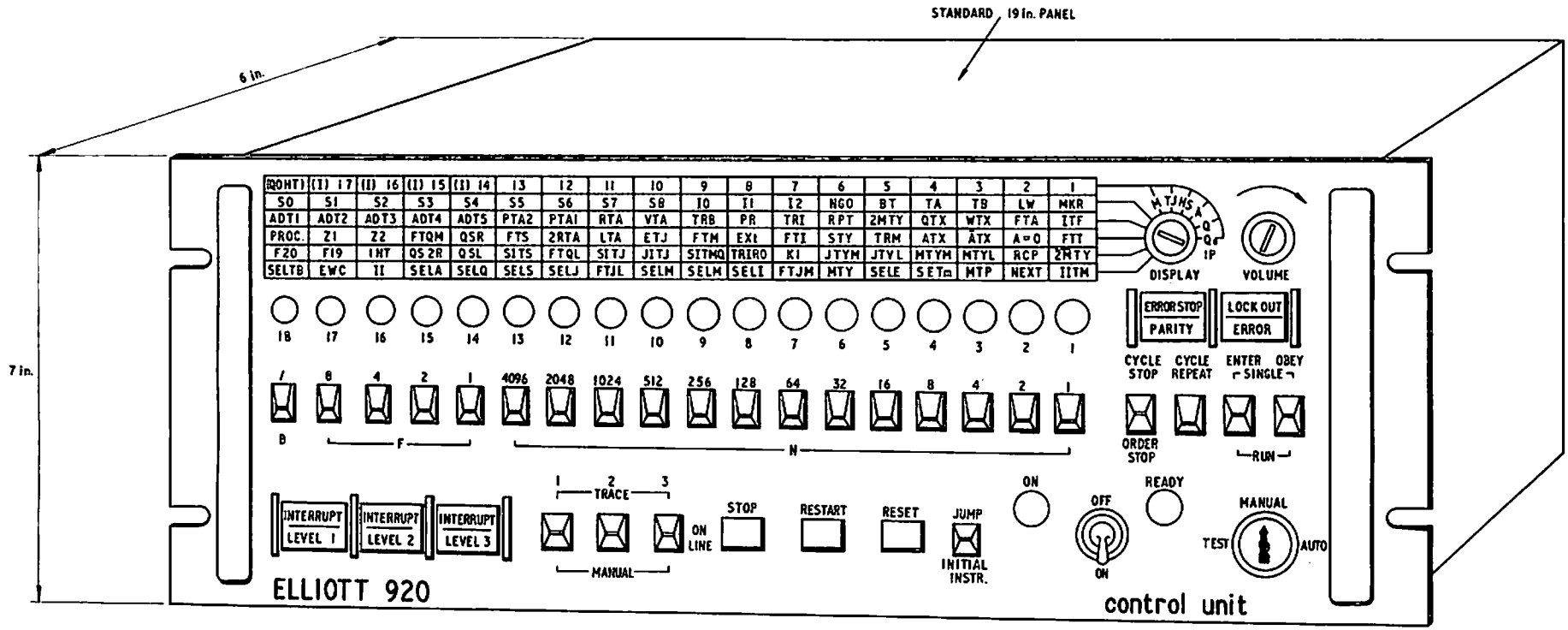
The 920C Control and Monitor Unit (MCC 40 and 41) has been designed based on Specification DEF 133 Class L1, which covers Ground Equipment, Protected.

6.2 Design Standard

The equipment is designed to meet the following tests:-

	Test	DEF 133 Clause
(i)	Visual Examination	6.1.
(ii)	Dry Heat	11.0. (A)
	Test A, temperature of +55°C, excluding measurement of surface temperatures. Carry out function test to DEF 133.	
(iii)	Damp Heat	11.1.
	Function unit to DEF 133	

	Test	DEF 133 Clause
(iii)	Damp Heat	11.1.
	Function unit to DEF 133	
(iv)	Low Temperature	12.0. (B)
	Test B, carry out function test after end of test.	
(v)	Damp Heat	11.1.
	Carry out function test to DEF 133.	
(vi)	Mould Growth	11.3.
	To be carried out on representative samples.	
(vii)	Visual Examination	6.1.



920C CONTROL AND MONITOR PANEL

SPECIFICATION

MCS 920C Marginal Test Unit

Catalogue No. MCC 52

1. General Description

The 920C Marginal Test Unit forms part of the MCS 920C Computer System, being required only when it is necessary to apply voltage and/or timing margins.

The unit is basically an item of test equipment, to check the performance of the computer under marginal conditions. It may also be used as an aid to fault finding.

The marginal test unit is a portable, free standing unit, the case size being 13" x 9" x $7\frac{1}{2}$".

2. Functional Specification

2.1 System Connections

The marginal test unit will have connected to it two cables, one being designed for connection to a power supply unit and the other for connection to a store unit. Both cables may be connected, or used independently.

2.1.1 Connection of the marginal test unit to a system power supply unit enables timing margins to be applied to the central processor, and in the case of a military power supply, voltage margins to the central processor and store units.

2.1.2 Connection of the marginal test unit to a store unit enables drive and threshold margins to be applied.

2.1.3 If connection as in section 2.1.1 is made to a power supply unit associated with the Interface Control Unit, then timing margins to the Interface Control Unit will be enabled, and in the case of a military power supply, voltage margins.

2.1.4 The timing margin signals for connection as in sections 2.1.1 and 2.1.3 will be routed via their respective power supply units, to avoid the necessity for extra cable connections between the system units and the marginal test unit. Two inter-connecting cables are supplied for use between the M.T.U. and a P.S.U., to accommodate military and commercial versions of the latter.

2.2 Margin Control

The marginal test unit is capable of applying up to eleven margins at a time. Each margin will be varied and set independently of the others, except the x and y drive margins for a store unit, which will be ganged together.

2.2.1 The unit is capable of applying individual margins to a maximum of ± 15% of their pre-margin operating level. The unit has an error at F.S.D. not greater than ± 2% of the pre-margin level. The indicating meter has a linear scale.

2.2.2 Each margin is applied and set using separate switches and potentiometers. A single rotary switch selects the margin to be displayed. Reference should be made to section 2.5 for details.

2.2.3 A single switch is provided for over-riding the protection circuits of the power supply unit, when applying voltage margins, to avoid inadvertent removal of the supply voltage.

This facility allows a function check to be applied to the system voltage protection circuits.

2.3 Indicators and Test Points

The unit provides 6 indicator lamps and 12 test points for indicating and monitoring, system supply and operating voltages. Reference should be made to section 2.5 for details. A seventh indicator lamp is provided to indicate Store Within Limits condition.

2.3.1 All the indicator lamps are 6 volts rating and are operated directly from the incoming lines. Where necessary, these lamps are provided with series resistors.

2.3.2 There is provision for 9 test points to monitor operating voltage levels associated with the store unit, and 3 test points for the power supply unit. Both these figures include a test point allotted to a 0 volt reference for each cable.

2.4 System Operation and Requirements

2.4.1 System Requirements

2.4.1.1 Each margin control circuit must be isolated from the other, except the "Timing" margin circuits which will operate from common input lines.

2.4.1.2 The internal wiring of the monitor indicators and test points must be wired directly to the input cable connector concerned.

2.4.1.3 The unit does not require a separate power supply source.

2.4.1.4 The unit frame must be earthed via the power supply unit cable.

2.4.2 Operation Procedure

2.4.2.1 Ensure all switches on the marginal test unit are in the normal or "off" position. Rotate each potentiometer to its mid position.

2.4.2.2 Connect the cable/s required to the store unit and/or power supply unit.

2.4.2.3 Rotate the margin selection switch to the required setting. The percentage margin meter is now enabled for the particular selection.

2.4.2.4 If the margin to be applied is to an output voltage line of a power supply unit, operate the "Protection Override" switch.

2.4.2.5 Operate the key switch appropriate for the selected margin. This allows the margin to be applied.

2.4.2.6 Rotate the potentiometer associated with the selected margin (and situated beneath the previously set key switch) until the required percentage of margin is indicated on the meter.

2.4.2.7 The above procedure is applicable for any other selected margin. A margin may be left applied while applying other margins, although only one of them may be indicated on the meter at any one time.

2.4.2.8 When using an external meter to monitor the actual voltage level of a margin, or any of the voltage levels available, the correct test point O volt reference must be used. Reference should be made to section 2.5.

2.4.2.9 When effecting any voltage margin the operator must shut down the system immediately should any power supply indicator fail to remain illuminated.

2.5 Margin, Indicator and Monitoring Facilities

The marginal test unit is able to apply a total of 11 margins, has 7 indicators and provides 10 monitor test points. The availability of these facilities with regard to military and commercial power supply units, central processor and interface control units, is detailed in tabular form in the Appendix.

3. Environmental Specification

3.1 General

The 920C Marginal Test Unit (MCC 52) has been designed based on Specification DEF.133 Class L.1, which covers Ground Equipment, Protected.

3.2 Design Standard

The equipment is designed to meet the following tests.

	Test	DEF.133 Clause
(i)	Visual Examination	6.1

(ii)	Dry Heat	11.0(A)
	Test A, temperature of +55°C. excluding measurement of surface temperatures.	
(iii)	Damp Heat	11.1
	Carry out function test to DEF.133.	
(iv)	Low Temperature	12.0(B)
	Test B, carry out function test after end of test.	
(v)	Damp Heat	11.1
	Carry out function test to DEF.133.	
(vi)	Mould Growth	11.3
	To be carried out on representative samples.	
(vii)	Visual Examination	6.1

4. Interface Specification

Introduction

The 920C Marginal Test Unit has two connectors, one of which provides the interface to a Power Supply Unit and the other to a Store Unit.

4.1 Power Supply Interface

The function and direction of the signals are given below.

4.1.1 Margin 1 Levels

To the M.T.U., five lines. These lines will provide the individual positive voltage levels for the four store and one processor (or I.C.U.) voltage margin control circuits.

4.1.2 Margin 3 Levels

To the M.T.U., five lines. These lines will provide the individual 0 volt level returns for 4.1.1.

4.1.3 Margin 2 Signals

From the M.T.U., five lines. These signal lines will force the five margins of 4.1.1. When the standing signal level is lowered a negative margin is obtained and when elevated a positive margin is obtained.

4.1.4 Timing Signals

From the M.T.U., two lines. These signal lines will force the two processor (or I.C.U.), timing margin control circuits. When the standing signal level is lowered a negative margin is obtained and when elevated a positive margin is obtained.

4.1.5 Protection Override

From the M.T.U., one line. This signal line when false will disable the power supply protection. The line is normally in the true or logic "1" state.

4.1.6 Voltage Monitor Levels

To the M.T.U., two lines. These lines will provide the voltage levels for two monitor test points.

4.2 Store Interface

The function and direction of the signals are given below.

4.2.1 Margin 1 Levels

To the M.T.U., four lines. These lines will provide the individual positive voltage levels for Drive, Inhibit and Threshold margin control circuits.

4.2.2 Margin 3 Levels

To the M.T.U., four lines. These lines will provide the individual 0 voltage level returns for 4.2.1.

4.2.3 Margin 2 Signals

From the M.T.U., four lines. These signal lines will force the four margins of 4.2.1. When the standing level is lowered a negative margin is obtained, and when elevated a positive margin is obtained.

4.2.4 Indicator and Monitor Levels

To the M.T.U., eight lines. These lines will provide the voltage levels for five indicators and eight monitor test points.

4.2.5 Store In Limits

To the M.T.U., one line. This signal line will be true when a store unit is within voltage and temperature limits. When true it will cause an indicator to illuminate. The line is normally in the true or logic 1 state.

4.3 Interface Connection Details

The details of the interconnections between a marginal test unit and a power supply unit and a store unit are given below:-

4.3.1 M.T.U./P.S.U. Connection Schedule: Plug A

M.T.U. fixed connector: Thorn PTO2E 20-39 PY
Cable free connector : Thorn PTO5A 20-39 SY

M.T.U. Plug Pin	Function		M.T.U. Plug Pin	Function	
A	Timing 1		R	Margin 1: +35v)	
B	Timing 2		S	Margin 2:)	Store
D	0V) Timing		T	Margin 3: 0V)	
E	+5v) supply		U	Margin 1: +5v)	
F	Margin 1: +5v)		V	Margin 2:)	C.P.
G	Margin 2:)	Store	W	Margin 3: 0V)	
H	Margin 3: 0V)		Y	Test point: -6v)	I.C.U.
J	Margin 1: -6v)		Z	Test point: +12v)	
K	Margin 2:)	Store	k	Protection Override (+VE)	
L	Margin 3: 0V)		m	Protection Override (-VE)	
M	Margin 1: +6v)		*p	Mains Earth	
N	Margin 2:)	Store			
P	Margin 3: 0V)				

* Connect to outer braid of cable form.

4.3.2 M.T.U. / Store Connection Schedule: Plug B

M.T.U. fixed connector: Thorn PTO2E 20-39 PW
Cable free connector : Thorn PTO5A 20-39 SW

M.T.U. Plug Pin	Function	M.T.U. Plug Pin	Function	
A	0V	P	Margin 1: +VE)	
B	+5v	R	Margin 2:)	X drive
C	-6v	S	Margin 3: -VE)	
D	+6Vwrt30V	T	Margin 1: +VE)	
E	+30v	U	Margin 2:)	Y drive
F	27-33V	V	Margin 3: -VE)	
G	+12v	W	Margin 1: +VE)	
H	Threshold	X	Margin 2:)	Threshold
L	Margin 1: +VE)	Y	Margin 3: -VE)	
M	Margin 2:) Inhibit	b	Store In Limits)	+VE
N	Margin 3: -VE)	c	Store In Limits)	-VE
		*n	0 volt	

* Connect to outer braid of cable form.

920C M.T.U. Facilities

Margins, Indicators and Test Points		M T U to Store MCC 14	M T U to P S U MCC 21	M T U to P S U MCC 24	M T U to P S U MCC 25
		6 PLA to 2 SKT D	6 PLB to 4 SKT E	6 PLB to 5 SKT E	6 PLB to 11 SKT C
Margins	A		Timing 1 C.P.	Timing 1 C.P.	Timing 1 I.C.U.
	B		Timing 2 C.P.	Timing 2 C.P.	Timing 2 I.C.U.
	V1		+5v C.P.		
	C	X Drive			
	D	Y Drive			
	E	Inhibit			
	F	Threshold			
	V2		+5v Store		
	V3		-6v Store		
	V4		+6v Store		
	V5		+30v Store		
Indicators	V1		+5v C.P.		
	V2	+5v Store			
	V3	-6v Store			
	V4	+6v Store			
	V5	+30v Store			
	E	27-33v Store			
	Store in Limits	Store in Limits			
Test Points	H	0V Store			
	V1		+5v C.P.	+5v C.P.	+5v I.C.U.
	V3	-6v Store			
	V4	+6wrt30v Store			
	V5	+30v Store			
	E	27-33v Store			
	G	+12v Store			
	F	+10v Thresh Store			
	V2	+5v Store			
	J				-6v I.C.U.
	K				+12v I.C.U.
	L		0V C.P.	0V C.P.	0V I.C.U.

SPECIFICATION

Paper Tape & Teleprinter Equipment

Catalogue Nos. MCC 66 A, B, C, D, E, F.

NOTE: These units are physically and functionally identical to 920B units (MCB 66), but the controller, MCC 66 A or F, contains circuit and component changes to permit the power supply to be switched on in a 920C system.

Cables

The cable from Plug CNA on the Controller logic unit to the Central Processor is changed to PL 322 C 9314, max length 10 ft.

322/SC70-82/8.68/1

MCS 920C Computer
SPECIFICATION

Paper Tape Readers, Punches & Teleprinters Catalogue Nos. MCC70-82.

The above units are identical to MCB items.